19-3217; Rev 0; 3/08

EVALUATION KIT AVAILABLE

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

General Description

The MAXQ7665A–MAXQ7665D smart systems-on-a-chip (SoC) are data-acquisition systems based on a microcontroller (µC). As members of the MAXQ® family of 16-bit, reduced instruction set computing (RISC) µCs, the MAXQ7665A–MAXQ7665D are ideal for low-cost, low-power, embedded applications such as automotive, industrial controls, and building automation. The flexible, modular architecture design used in these µCs allows development of targeted products for specific applications with minimal effort.

The MAXQ7665A–MAXQ7665D incorporate a high-performance 16-bit RISC core, a 12-bit 500ksps SAR ADC with a programmable gain amplifier (PGA), and a full CAN 2.0B controller supporting transfer rates up to 1Mbps. These devices include a 12-bit DAC with a buffered voltage output and on-chip oscillator circuitry to operate from an external high frequency (8MHz) crystal. There is also a built-in internal RC oscillator as an alternative to using an external crystal. The MAXQ7665A–MAXQ7665D contain an internal temperature sensor to measure die temperature and a remote temperature-sensor driver. The analog functions and digital I/O are powered from a +5V supply, while the internal digital core is powered from +3.3V, which can be supplied by an on-chip linear regulator. These devices also include a dual power-supply supervisor with reset and a JTAG interface for in-system programming and debugging. The 16-bit RISC µC includes up to 128KB (64K x 16) of flash memory and 512 bytes (256 x 16) of RAM.

The MAXQ7665A–MAXQ7665D are available in a 7mm x 7mm 48-pin TQFN package and are specified to operate from -40°C to +125°C.

Applications

Automotive Steering Sensors

CAN- and LIN-Based Automotive Sensors

Industrial Control

Features

♦ **High-Performance, Low-Power, 16-Bit RISC Core**
- DC-to-8MHz Operation, Approaching 1MIPS per MHz
- Low Power (< 3mA/MIPS, DV_{DD} = +3.3V)
- 16-Bit Instruction Word, 16-Bit Data Bus
- 33 Instructions (Most Require Only One Clock Cycle)
- 16-Level Hardware Stack
- Three Independent Data Pointers with Automatic Increment/Decrement

♦ **Program and Data Memory**
- Up to 128KB (64K x 16) Internal Flash
- 512 Bytes (256 x 16) Internal RAM

♦ **Smart Analog Peripherals**
- Low-Power, Eight Differential-Channel, 12-Bit, 500ksps ADC
- Programmable-Gain Amplifier, Software-Selectable Gain: 1V/V, 2V/V, 4V/V, 8V/V, 16V/V, 32V/V
- 12-Bit DAC with Buffered Voltage Output
- External References for ADC and DAC
- Internal (Die) and External Diode Temperature Sensing

♦ **Timer/Digital I/O Peripherals**
- Full CAN 2.0B Controller
  - 15 Message Centers (256-Byte Dual Port Memory)
  - Programmable Bit Rates from 10kbps to 1Mbps
  - Standard 11-Bit or Extended 29-Bit Identification Modes
  - Two Data Masks and Associated IDs for DeviceNET™, SDS and Other Higher Layer CAN Protocols
  - External Transmit Disable for Autobaud
  - SIESTA Low-Power Mode
  - Wake-Up on CANRXD Edge Transition
- UART (LIN) with User-Programmable Baud Rate
- 16 x 16 Hardware Multiplier with 48-Bit Accumulator, Single Clock Cycle Operation
- Three 16-Bit (or Six 8-Bit) Programmable Timer/Counter/PWM
- Eight General-Purpose, Digital I/O Pins, with External Interrupt Capability
- All Interrupts Can Be Used as a Wake-Up

♦ **Crystal/Clock Module**
- Internal Oscillator for Use with External Crystal
- On-Chip RC Oscillator Eliminates External Crystal
- External Clock-Source Operation
- Programmable Watchdog Timer

♦ **Power-Management Module**
- Power-On Reset (POR)
- Power-Supply Supervisor/Brownout Detection for Digital I/O and Digital Core Supplies
- On-Chip +3.3V, 50mA Linear Regulator

♦ **JTAG Interface**
- Extensive Debug and Emulation Support
- In-System Test Capability
- Flash-Memory-Program Download
- Software Bootstrap Loader for Flash Programming

♦ **Ultra-Low-Power Consumption**
- Low-Power, Divide-by-256 PMM Mode
- Stop Mode

Ordering Information/Selector Guide and Pin Configuration appear at end of data sheet.

MAXQ is a registered trademark of Maxim Integrated Products, Inc.
DeviceNet is a trademark of Open DeviceNet Vendor Association, Inc.

Note: *Some revisions of this device may incorporate deviations from published specifications known as errata. Multiple revisions of any device may be simultaneously available through various sales channels. For information about device errata, go to:* ***www.maxim-ic.com/errata****.*

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

ABSOLUTE MAXIMUM RATINGS

DV_{DD} to DGND, AGND, or GNDIO .....-0.3V to +4V
DGND to GNDIO or AGND.....-0.3V to +0.3V
DV_{DDIO} to DGND, AGND, or GNDIO .....-0.3V to +6V
AV_{DD} to DGND, AGND, or GNDIO.....-0.3V to +6V
Digital Inputs/Outputs to DGND, AGND, or GNDIO
.....-0.3V to (DV_{DDIO} + 0.3V)
Analog Inputs/Outputs to DGND, AGND, or GNDIO
.....-0.3V to (AV_{DD} + 0.3V)
$\overline{RESET}$, XIN, XOUT to DGND, AGND, or GNDIO
.....-0.3V to (DV_{DD} + 0.3V)
Continuous Current into Any Pin.....±50mA
Continuous Power Dissipation (T_A = +70°C)
48-Pin TQFN (derate 40mW/°C above +70°C) 3200mW
Operating Temperature Range .....-40°C to +125°C
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
POWER REQUIRMENTS						
Supply Voltage Range	DV_{DD}	Safe mode (RC/2 = 3.8MHz)	2.7	3.3	3.6	V
		Normal mode	3.0	3.3	3.6	
	AV_{DD}		4.75	5.0	5.25	
	DV_{DDIO}		4.75	5.0	5.25	
AV_{DD} Supply Current	I_{AVDD}	Shutdown (Note 2)		0.1	10	µA
		All analog functions enabled		6.7	8	mA
Analog Module Subfunction Incremental Supply Current		ADC enabled, f_{ADC} = 1ksps, f_{SYSCLK} = 8MHz		4.2		µA
		ADC enabled, f_{ADC} = 500ksps, f_{SYSCLK} = 8MHz		1890		
		DAC enabled (zero scale)		305		
		Internal temperature sensor enabled		502		
		Additional current when one or more of the ADC, DAC, and/or temperature sensor is enabled (only counted once)		128		
		PGA enabled		4.5		mA
DV_{DD} Supply Current	I_{DVDD}	CPU in stop mode, all peripherals disabled		3	20	µA
		Medium-speed mode (Note 3)			5	mA
		High-speed mode (Note 4)			28	
		Low-speed mode (Note 5)			2	
		Flash erase or write mode		35	50	
DV_{DD} Module Subfunction Incremental Supply Current		DV_{DD} supervisor and brownout monitor		2		µA
		HF crystal oscillator		150		
		Internal RC oscillator		200		
DV_{DDIO} Supply Current	I_{DVDDIO}	All digital I/Os static at GND or DV_{DDIO}			10	µA
		(Note 6)			1000	

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
MEMORY SECTION						
Flash Memory Size		MAXQ7665A		128		KB
		MAXQ7665B		64		
		MAXQ7665C		48		
		MAXQ7665D		32		
Flash Erase/Write Endurance		DV_{DD} = +3V, at +25°C		1		MCycles
		DV_{DD} = +3V, at +85°C		100		kCycles
		DV_{DD} = +3V, at +125°C		100		kCycles
Flash Erase Timing		One sector		0.7	15	s
Flash Program Timing		Single word		11	360	µs
		Entire flash		1.5	4.5	s
Flash Data Retention Time		T_A = +125°C, single write	20			Years
		First 100,000 cycles at +25°C, then retention tested at T_A = +125°C	10			
RAM Memory Size				512		Bytes
Utility ROM Size				4096		Words
ANALOG SENSE PATH						
Resolution	N_{ADC}	No missing codes	12			Bits
Integral Nonlinearity	INL_{ADC}	Gain = 1, bipolar mode, V_{IN} = ±2500mV, 500ksps		±0.5	±4.0	LSB
		Gain = 8, unipolar mode, V_{IN} = +400mV, 142ksps		±2.0		
		Gain = 16, bipolar mode, V_{IN} = ±156mV, 142ksps		±2.0	±4.0	
		Gain = 32, bipolar mode, V_{IN} = ±50mV, 142ksps		±2.0		
Differential Nonlinearity	DNL_{ADC}	Gain = 1, bipolar, V_{IN} = ±2500mV, 500ksps			±1.0	LSB
		Gain = 16, bipolar, V_{IN} = ±156mV, 142ksps			±1.0	
		All other gain settings		±0.6		
Offset Error		Input referred		±2.5	±5	mV
Offset-Error Temperature Coefficient				±8		µV/°C
Zero-Code Error		Bipolar, differential measurement of error for ideal ADC output of 0x000		±2.5		mV
Gain Error		Exclude offset and reference error	-1.0		+1.0	%
Gain-Error Temperature Coefficient				±8.5		ppm/°C
Signal-to-Noise Plus Distortion	SINAD	PGA gain = 1V/V		-71		dB
Total Harmonic Distortion	THD	PGA gain = 1V/V		-85		dB

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Spurious-Free Dynamic Range	SFDR	PGA gain = 1V/V			-91		dB
Conversion Clock Frequency	f_{ADCCLK}	f_{SYSCLK} = 8MHz		0.5		8.0	MHz
Sample Rate	f_{SAMPLE}	PGA gain = 1V/V, $R_{SOURCE} \le 1k\Omega$				500	ksps
		Any PGA gain setting > 1V/V, $R_{SOURCE} \le 5k\Omega$				142	
Conversion Time	t_{CONV}	t_{ACQ} plus 13 ADCCLK cycles at 8MHz				t_{ACQ} + 1.625	µs
Channel/Gain Select Plus Conversion Time		PGA gain = 1V/V, $R_{SOURCE} \le 1k\Omega$				2	µs
		Any PGA gain setting, $R_{SOURCE} \le 5k\Omega$				7	
Track-and-Hold Acquisition Time	t_{ACQ}	PGA gain = 1V/V, $R_{SOURCE} \le 1k\Omega$				375	ns
		Any PGA gain setting > 1V/V, $R_{SOURCE} \le 5k\Omega$				5	µs
Turn-On Time	t_{RECOV}				5		µs
Aperture Delay					30		ns
Aperture Jitter					50		ps_{P-P}
Input-Voltage Range		Unipolar mode	PGA gain = 1	0		AV_{DD}	V
			PGA gain = 2	0		1.6	
			PGA gain = 4	0		0.8	
			PGA gain = 8	0		0.4	
			PGA gain = 16	0		0.2	
			PGA gain = 32	0		0.1	
		Bipolar mode, AIN+ to AIN-	PGA gain = 1	$-V_{REFADC}/2$		$+V_{REFADC}/2$	
			PGA gain = 2	$-V_{REFADC}/4$		$+V_{REFADC}/4$	
			PGA gain = 4	$-V_{REFADC}/8$		$+V_{REFADC}/8$	
			PGA gain = 8	$-V_{REFADC}/16$		$+V_{REFADC}/16$	
			PGA gain = 16	$-V_{REFADC}/32$		$+V_{REFADC}/32$	
			PGA gain = 32	$-V_{REFADC}/64$		$+V_{REFADC}/64$	
Absolute Input-Voltage Range				AGND		AV_{DD}	V
Input Leakage Current		AIN15–AIN0			±20		nA
Small-Signal Bandwidth (-3dB)		V_{IN} x gain = $100mV_{P-P}$	PGA gain = 1		180		MHz
			PGA gain = 2		140		
			PGA gain = 4		120		
			PGA gain = 8		100		
			PGA gain = 16		82		
			PGA gain = 32		80		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Large-Signal Bandwidth (-3dB)		V_{IN} x gain = 3.2V_{P-P}	PGA gain = 1		180		kHz
			PGA gain = 2		140		
			PGA gain = 4		120		
			PGA gain = 8		100		
			PGA gain = 16		82		
			PGA gain = 32		80		
Input Capacitance		Single-ended, any input of AIN0 to AIN15	PGA gain = 1		13.6		pF
			PGA gain = 2		2		
			PGA gain = 4		4		
			PGA gain = 8		8		
			PGA gain = 16		16		
			PGA gain = 32		32		
Crosstalk Between Channels	V_{CT}	AIN15–AIN0, V_{IN} = 1V_{P-P}, 10kHz, R_{SOURCE} = 5kΩ			-80		dB
Input Common-Mode Rejection Ratio	CMRR	AIN15–AIN0 (bipolar, differential), V_{CM} = 100mV to 4.5V		-70	-90		dB
Power-Supply Rejection Ratio	PSRR	AV_{DD} = +4.75V to +5.25V		67	75		dB
DAC SECTION (DACOUT, R_L = 5kΩ and C_L = 100pF)							
Resolution	N_{DAC}	Guaranteed monotonic		12			Bits
Differential Nonlinearity	DNL_{DAC}	Code 147h to E68h			±0.4	±1	LSB
Integral Nonlinearity	INL_{DAC}	Code 147h to E68h			±0.5	±4	LSB
Offset Error		Reference to code 040h			±2.5	±30	mV
Offset-Error Temperature Coefficient					±5		µV/°C
Gain Error		Excludes reference error, tested at E68h			±3	±20	LSB
Gain-Error Temperature Coefficient		Excludes offset and reference drift; calculated from FSR			±2		ppm of FSR/°C
DAC Output Range		No load		0		V_{REFDAC}	V
DC Output Impedance	Z_{OUT}	Termination resistance to AGND	DAC enabled		0.5		Ω
			Power-down mode		105		kΩ
Output Slew Rate		400h to C00h code swing, rising or falling			0.6		V/µs
Output Settling Time		147h to E68h code swing, settling to ±0.5 LSB (Note 7)			8	15	µs
Output Short-Circuit Current		Short to AGND			-27		mA
		Short to AV_{DD}			46		

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DAC Glitch Impulse		From 7FFh to 800h			12		nV•s
DAC Power-On Time		Excluding reference, settling to ±0.5 LSB			14		µs
Power-Supply Rejection		AV_{DD} step from +4.75V to +5.25V			62		µV/V
Output Noise		C_L = 200pF			200		$µV_{RMS}$
EXTERNAL REFERENCE INPUTS							
REFADC Input-Voltage Range				1.0	5.0	AV_{DD}	V
REFDAC Input-Voltage Range				0	5.0	AV_{DD}	V
REFDAC Input Impedance					200		kΩ
REFADC Leakage Current		ADC disabled			1		µA
TEMPERATURE SENSOR (Remote NPN Transistor 2N3904)							
Temperature Error		Internal diode	T_A = +25°C		±1		°C
			T_A = -30°C to +85°C		±2		
			T_A = -40°C to +125°C		±5		
		External diode, differential configuration (Note 8)	T_A = +25°C, T_{RJ} = +25°C		±2		
			T_A = -30°C to +85°C, T_{RJ} = +25°C		±3		
			T_A = -40°C to +125°C, T_{RJ} = +25°C		±3		
			T_A = -30°C to +85°C, T_{RJ} = -30°C to +85°C		±3		
			T_A = -40°C to +125°C, T_{RJ} = -40°C to +125°C		±5		
Internal (Die) or External Temperature Measurement Error vs. V_{REFADC} Variation					0.095		°C/mV
External Diode Source Current		High level			74.7		µA
		Low level			4		
External Diode Drive Current Ratio					18.7:1		µA/µA
Conversion Time		f_{ADCCLK} = f_{SYSCLK} = 8MHz, no interrupts, internal utility ROM tempConv			70		µs
Temperature Resolution		12-bit ADC			0.125		°C/LSB
+3.3V LINEAR REGULATOR (C_{DVDD} = 4.7µF)							
DV_{DDIO} Input-Voltage Range				4.25	5.0	5.25	V
DV_{DD} Output Voltage		$\overline{REGEN}$ = GNDIO		3.0	3.4	3.6	V
DV_{DD} Input-Voltage Range		$\overline{REGEN}$ = DV_{DDIO}		3.0		3.6	V
No-Load Quiescent Current		CPU in sleep mode; all digital peripherals disabled			15		µA
Output Short-Circuit Current		Short to DGND			110		mA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SUPPLY VOLTAGE SUPERVISORS AND BROWNOUT DETECTION							
DV_{DD} Voltage-Supervisor Reset Rising Threshold		Power-on default, DV_{DD} voltage rising (Note 9)		2.70		2.99	V
DV_{DD} Voltage-Supervisor Brownout Reset Falling Threshold	V_{VDBR}	DV_{DD} voltage falling, firmware selectable, measured with CPU active at 8MHz (Note 10)	VDBR = 00b (default)	2.70		2.99	V
			VDBR = 01b	2.77		3.06	
			VDBR = 10b	2.84		3.13	
			VDBR = 11b	2.91		3.20	
Software-Selectable DV_{DD} Voltage-Supervisor Brownout Interrupt Falling Threshold	V_{VDBI}	DV_{DD} voltage falling, firmware selectable, measured with CPU active at 8MHz (Note 11)	VDBI = 00b (default)	2.77		3.06	V
			VDBI = 01b	2.84		3.13	
			VDBI = 10b	2.91		3.20	
			VDBI = 11b	2.99		3.27	
DV_{DDIO} Voltage-Supervisor Brownout Interrupt Threshold	V_{VIOBI}	DV_{DDIO} voltage falling, firmware selectable, measured with CPU active at 8MHz (Note 12)	VIOBI = 00b (default)	4.25		4.74	V
			VIOBI = 01b	4.30		4.79	
			VIOBI = 10b	4.35		4.84	
			VIOBI = 11b	4.40		4.89	
Voltage-Supervisor Hysteresis		DV_{DD}, DV_{DDIO}			1		%
DV_{DD} Brownout-Interrupt to Brownout Reset Falling Threshold		Voltage difference between V_{VDBI} and V_{VDBR}, time allowing software clean-up before reset asserted, VDBI = 11b and VDBR = 10b		155			mV
Voltage Monitor Range		DV_{DD}		1.0		3.6	V
		DV_{DDIO}		0		5.25	
DV_{DD} Ramp-Up Rate		DV_{DD} must rise faster than this rate between +2.7V and +3.0V		35			mV/ms
$\overline{RESET}$ Hold Time		After DV_{DD} rises above the V_{VDBR} voltage trip threshold			16		ms
CAN INTERFACE							
CAN Baud Rate		CANCLK = 8MHz				1	Mbps
CANCLK Mean Frequency Error		50ppm external crystal error, 8MHz crystal			60		ppm
CANCLK Total Frequency Error		50ppm external crystal error, 8MHz crystal, clock divided and measured over 500µs interval, mean plus peak cycle jitter			< 0.5		%
HIGH-FREQUENCY CRYSTAL OSCILLATOR							
Clock Frequency		Using external crystal		1.00		8.12	MHz
		External clock source				8.12	
Crystal Oscillator Startup Time		8MHz crystal			10		ms
External Clock Input Duty Cycle		Ratio high-to-low or low-to-high		45		55	%

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Crystal Oscillator Stability		Excluding crystal		3		ppm/V
XIN Input Load Capacitance		HFIC = 00b (default)		7		pF
		HFIC = 01b		18		
		HFIC = 10b		27		
		HFIC = 11b		34		
XOUT Output Load Capacitance		HFOC = 00b (default)		6		pF
		HFOC = 01b		17		
		HFOC = 10b		27		
		HFOC = 11b		34		
XIN Input Low Voltage		Driven with external clock source			0.3 x DV_{DD}	V
XIN Input High Voltage		Driven with external clock source	0.7 x DV_{DD}			V
INTERNAL RC OSCILLATOR						
Oscillator Frequency			7.0	7.6	8.0	MHz
Oscillator Startup Time				10		µs
Oscillator Jitter				2.7		ns
UART (LIN) INTERFACE (UTX, URX)						
UART Baud Rate			0		2	Mbps
Minimum LIN Mode Operation					1	kbps
Maximum LIN Mode Operation			20			kbps
UART Baud Rates Error		Crystal clock source	-0.5		+0.5	%
		Using internal RC oscillator before autobaud	-14.0		+14.0	
		Using internal RC oscillator after autobaud	-0.5		+0.5	
RESET ($\overline{RESET}$)						
$\overline{RESET}$ Internal Pullup Resistance		Pullup to DV_{DD}		305		kΩ
$\overline{RESET}$ Output Voltage		High, $\overline{RESET}$ deasserted, no load	0.9 x DV_{DD}			V
		Low, $\overline{RESET}$ asserted, no load			0.4	
$\overline{RESET}$ Input High Voltage			0.7 x DV_{DD}			V
$\overline{RESET}$ Input Low Voltage					0.3 x DV_{DD}	V
DIGITAL INPUTS (P0._, CANRXD, URX, $\overline{REGEN}$)						
Input Low Voltage					0.3 x DV_{DDIO}	V
Input High Voltage			0.7 x DV_{DDIO}			V
Input Hysteresis				500		mV
Input Leakage Current		V_{IN} = GNDIO or DV_{DDIO}, pullup disabled	-1	±0.01	+1	µA

ELECTRICAL CHARACTERISTICS (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{SYSCLK} = 8MHz, V_{REFDAC} = V_{REFADC} = +5V, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Resistance		Pullup to DV_{DDIO}		400		kΩ
Input Capacitance		V_{IN} = GNDIO or DV_{DDIO}		15		pF
DIGITAL OUTPUTS (P0._, CANTXD, UTX)						
Output Low Voltage		I_{SINK} = 1.6mA			0.4	V
Output High Voltage		I_{SOURCE} = 1.6mA	DV_{DDIO} - 0.5			V
Output Leakage Current		I/O pins, three-state	-1	±0.01	+1	µA
Output Capacitance		I/O pins, three-state		15		pF
Output Short-Circuit Current		Short to DV_{DDIO} = +5.25V		29		mA
		Short to GNDIO		28		

Note 1: All devices are 100% production tested at T_A = +25°C.

Note 2: All analog functions disabled and all digital inputs connected to supply or ground.

Note 3: Medium-speed mode: CPU and one timer running at 1MHz from an external crystal oscillator, all other peripherals disabled, all digital I/Os static at DV_{DDIO} or GNDIO.

Note 4: High-speed mode: CPU and three timers running at 8MHz from an external crystal oscillator, CAN enabled and communicating at 500kbps, all other peripherals disabled, all digital I/Os static at DV_{DDIO} or GNDIO.

Note 5: Low-speed mode: CPU and one timer running from an external crystal oscillator in PMM mode, all other peripherals disabled, all digital I/Os static at DV_{DDIO} or GNDIO.

Note 6: CAN transmitting at 500kbps, one timer output at 500kHz, all active I/Os are loaded with 20pF capacitor, all remaining digital I/Os are at DV_{DDIO} or GNDIO.

Note 7: Guaranteed by design and characterization.

Note 8: Based on diode ideality factor of 1.008.

Note 9: DV_{DD} must rise above V_{VDBR} for $\overline{RESET}$ to become deasserted. **Caution:** Operation is not guaranteed for DV_{DD} below +2.7V (utility ROM) or +3.0V (flash).

Note 10: $\overline{RESET}$ is asserted if DV_{DD} falls below V_{VDBR}. **Caution:** Operation is not guaranteed for DV_{DD} below +2.7V (utility ROM) or +3.0V (flash).

Note 11: An interrupt is generated if DV_{DD} falls below V_{VDBI}. **Caution:** Operation is not guaranteed for DV_{DD} below +2.7V (utility ROM) or +3.0V (flash).

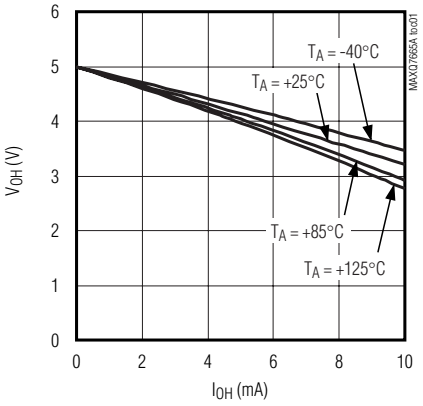
Note 12: An interrupt is generated if DV_{DDIO} falls below V_{VIOBI}. **Caution:** Operation is not guaranteed if DV_{DDIO} or AV_{DD} is below 4.75V, except for the DV_{DDIO} brownout monitor and +3.3V linear regulator, that still operate down to 0V and +4.25V, respectively.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

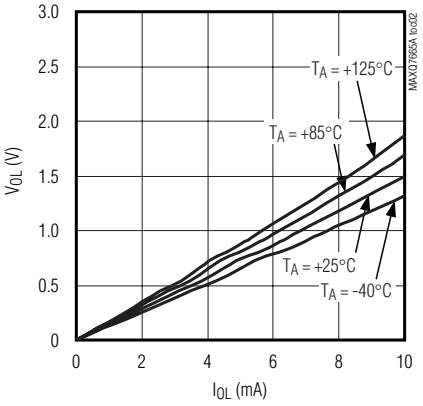
Typical Operating Characteristics

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

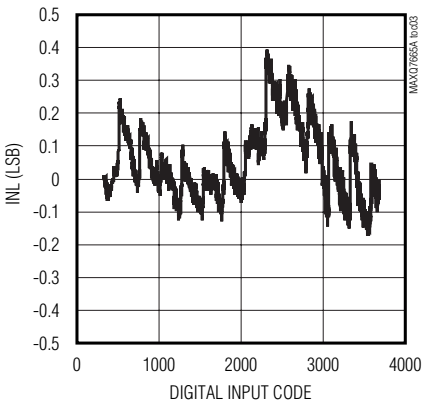
GPO._ OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



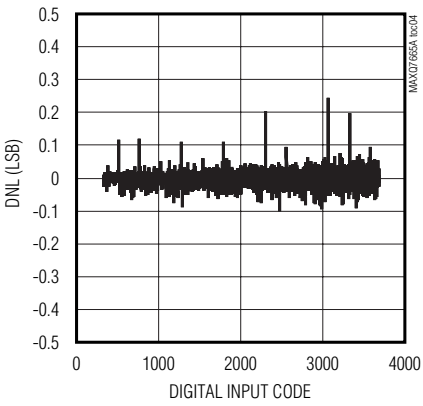
GPO._ OUTPUT LOW VOLTAGE vs. SINK CURRENT



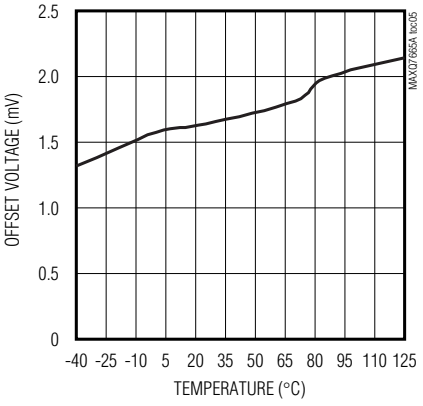
DAC INL vs. INPUT CODE (REFDAC = +5V)



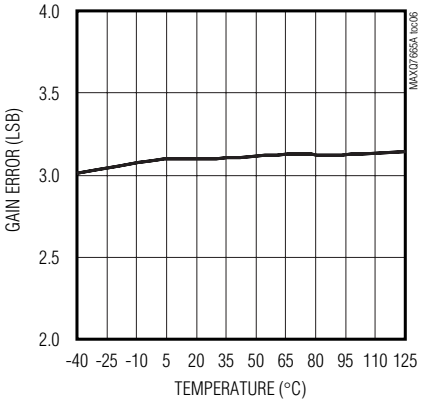
DAC DNL vs. INPUT CODE (REFDAC = +5V)



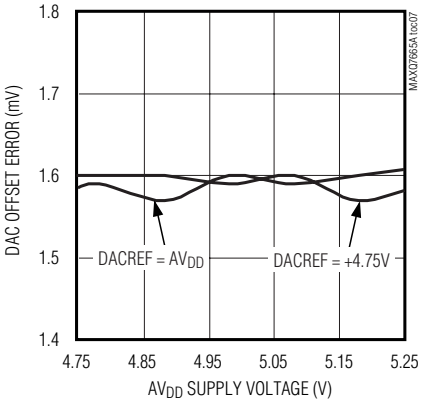
DAC OFFSET VOLTAGE vs. TEMPERATURE



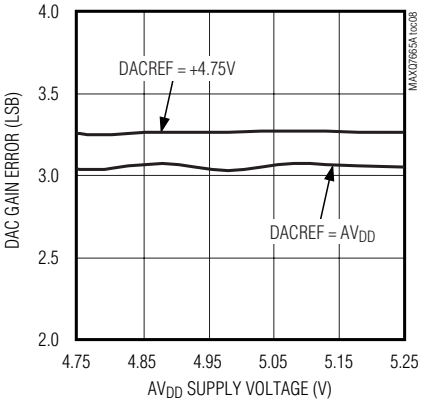
DAC GAIN ERROR vs. TEMPERATURE



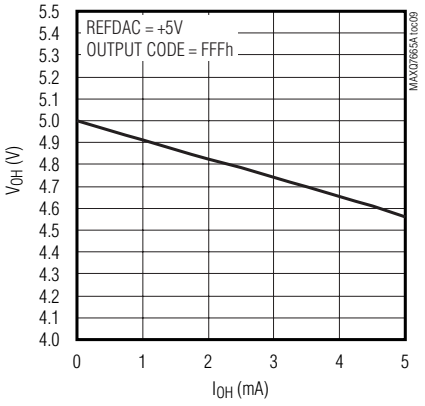
DAC OFFSET ERROR vs. AV_{DD} SUPPLY VOLTAGE



DAC GAIN ERROR vs. AV_{DD} SUPPLY VOLTAGE



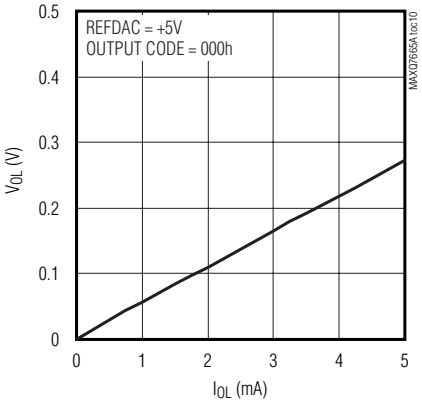
DACOUT OUTPUT HIGH VOLTAGE vs. SOURCE CURRENT



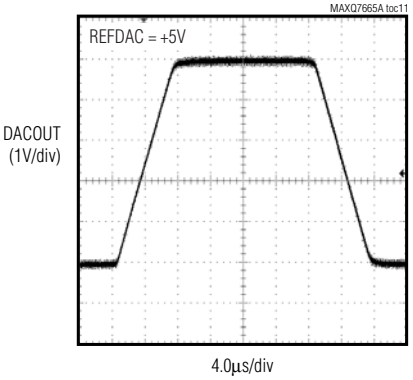
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

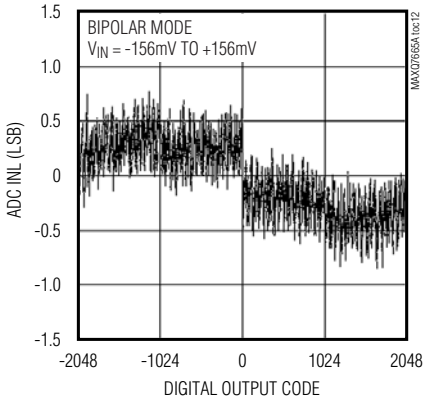
DACOUT OUTPUT LOW VOLTAGE vs. SINK CURRENT



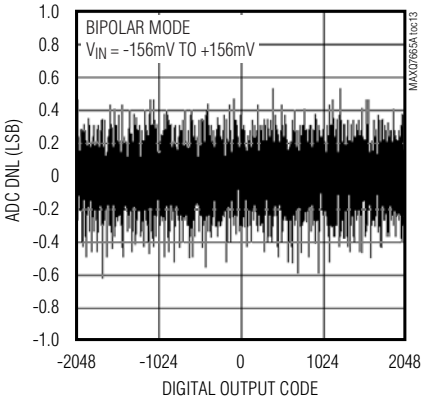
DACOUT LARGE-SIGNAL STEP RESPONSE (CODE 000h TO FFFh)



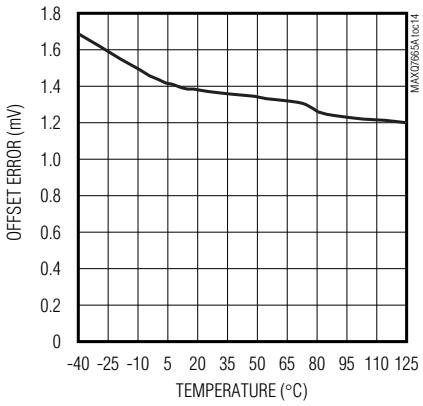
ADC INL vs. OUTPUT CODE (REFADC = +5V, 142ksps, PGA GAIN = 16)



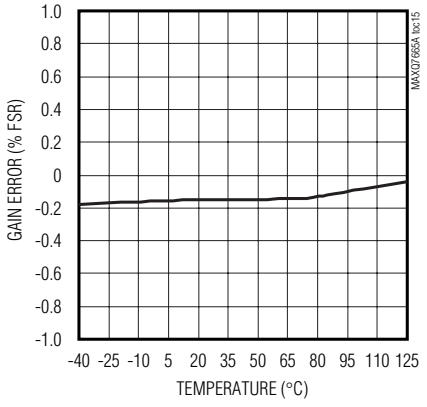
ADC DNL vs. OUTPUT CODE (REFADC = +5V, 142ksps, PGA GAIN = 16)



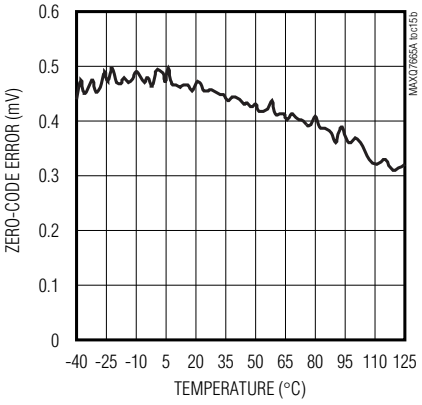
ADC/PGA OFFSET ERROR (GAIN = 16) vs. TEMPERATURE



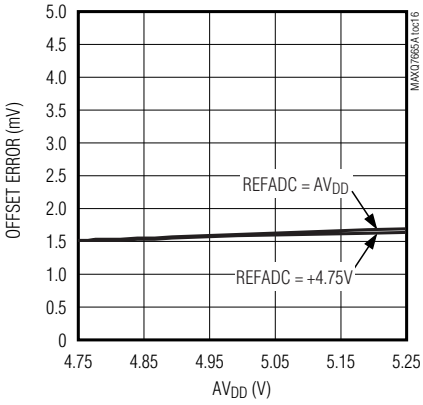
ADC/PGA GAIN ERROR (GAIN = 16) vs. TEMPERATURE



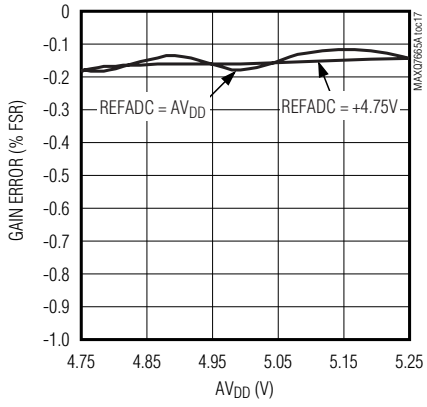
ADC BIPOLAR ZERO-CODE ERROR vs. TEMPERATURE



ADC/PGA OFFSET ERROR (GAIN = 16) vs. AV_{DD} SUPPLY VOLTAGE



ADC/PGA GAIN ERROR (GAIN = 16) vs. AV_{DD} SUPPLY VOLTAGE

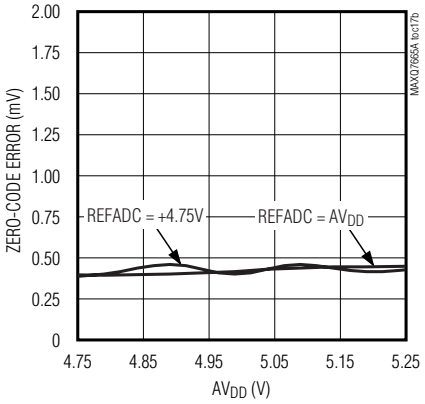


16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

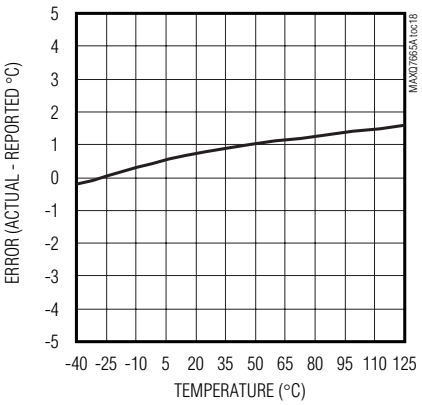
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

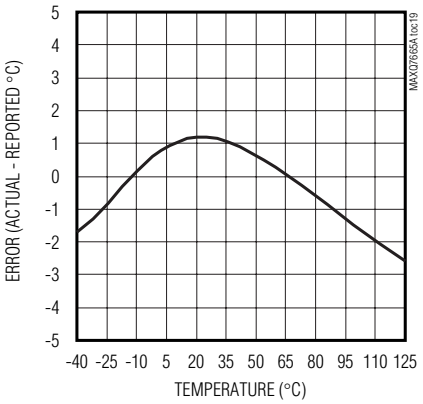
ADC/PGA ZERO-CODE ERROR (GAIN = 16) vs. AV_{DD} SUPPLY VOLTAGE



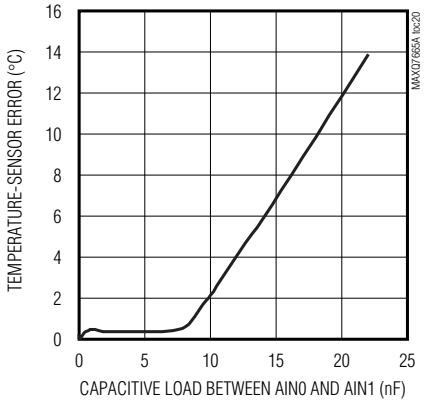
INTERNAL DIODE TEMPERATURE-SENSOR ERROR vs. TEMPERATURE



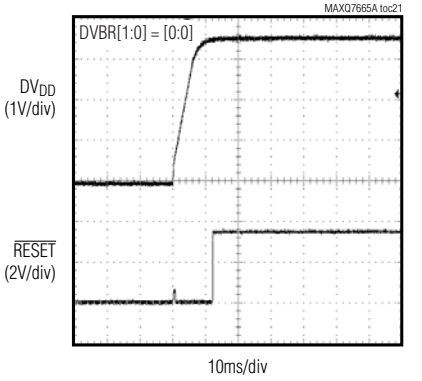
EXTERNAL DIODE TEMPERATURE-SENSOR ERROR vs. TEMPERATURE



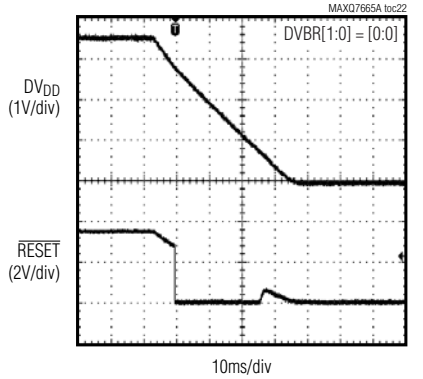
REMOTE TEMPERATURE-SENSOR ERROR DUE TO CAPACITIVE LOADING



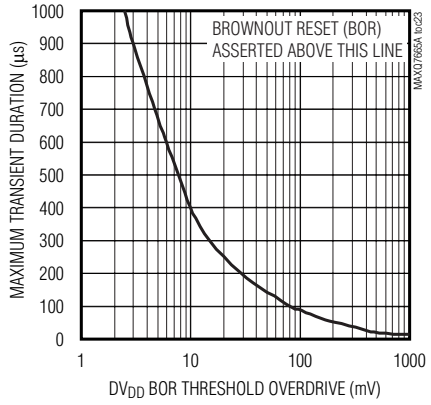
DV_{DD}, $\overline{RESET}$ POWER-UP CHARACTERISTICS



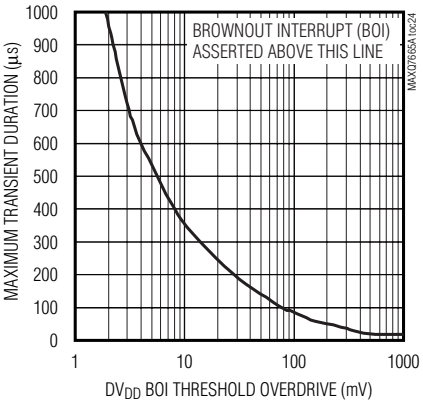
DV_{DD}, $\overline{RESET}$ POWER-DOWN CHARACTERISTICS



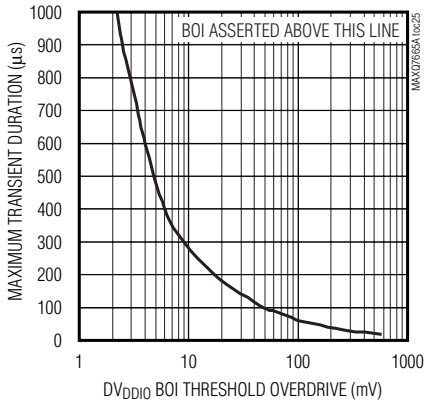
MAXIMUM DV_{DD} TRANSIENT DURATION vs. BOR THRESHOLD OVERDRIVE



MAXIMUM DV_{DD} TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



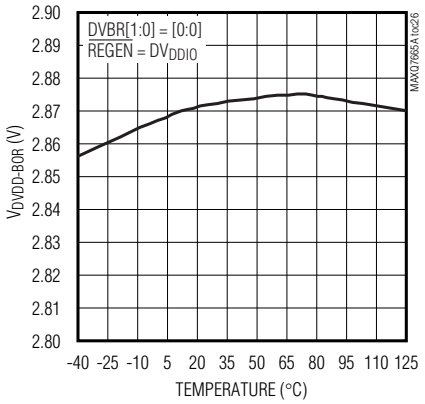
MAXIMUM DV_{DDIO} TRANSIENT DURATION vs. BOI THRESHOLD OVERDRIVE



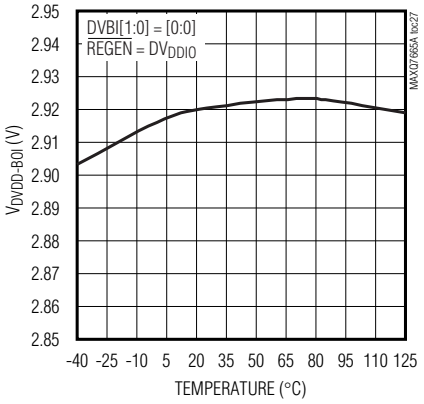
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

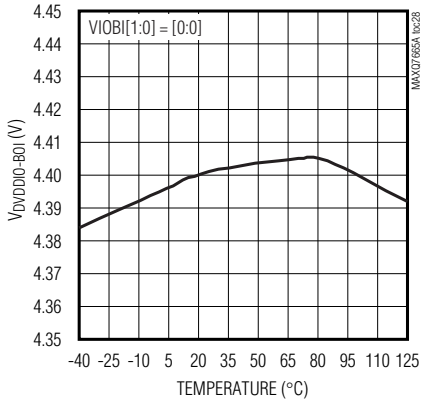
DV_{DD} BOR THRESHOLD VOLTAGE vs. TEMPERATURE



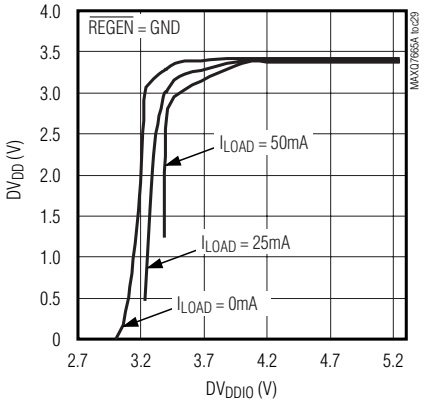
DV_{DD} BOI THRESHOLD VOLTAGE vs. TEMPERATURE



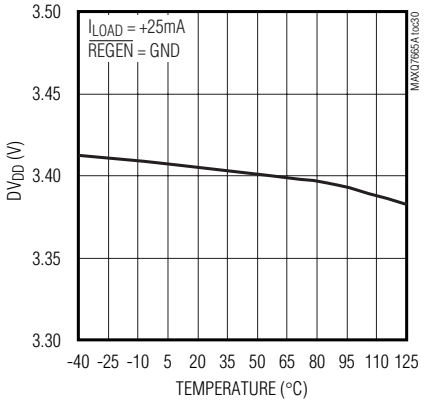
DV_{DDIO} BOI THRESHOLD VOLTAGE vs. TEMPERATURE



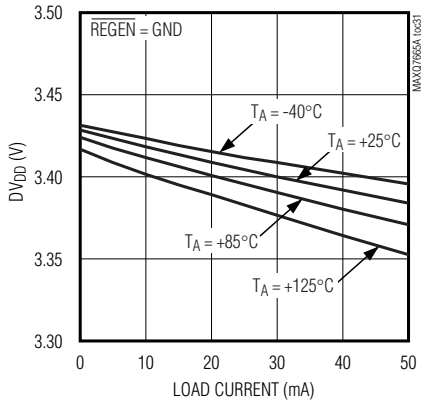
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE vs. DV_{DDIO} SUPPLY VOLTAGE



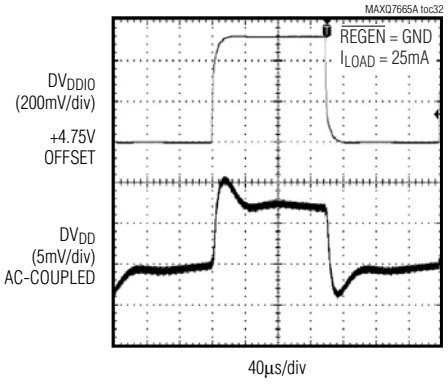
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE vs. TEMPERATURE



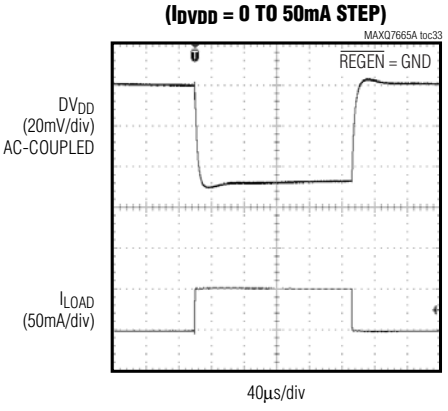
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE vs. LOAD CURRENT



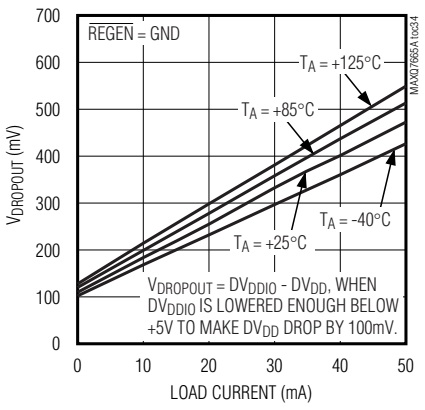
DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE LINE TRANSIENT (DV_{DDIO} = +4.75V TO +5.25V STEP)



DV_{DD} LINEAR REGULATOR OUTPUT VOLTAGE LOAD TRANSIENT (I_{DVDD} = 0 TO 50mA STEP)



DV_{DD} LINEAR REGULATOR DROPOUT VOLTAGE vs. LOAD CURRENT

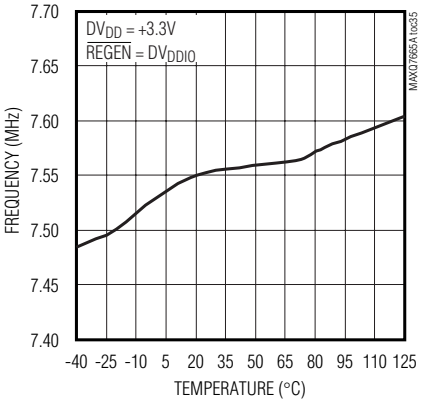


16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

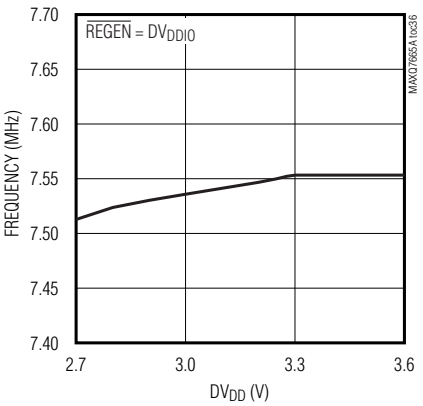
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

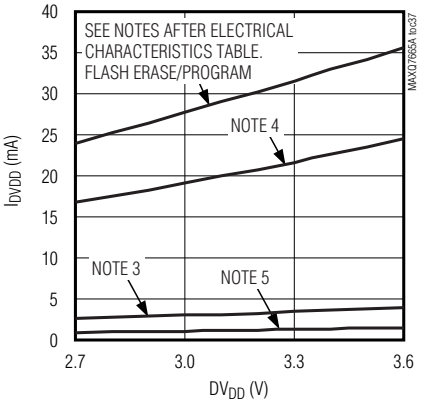
RC OSCILLATOR OUTPUT FREQUENCY vs. TEMPERATURE



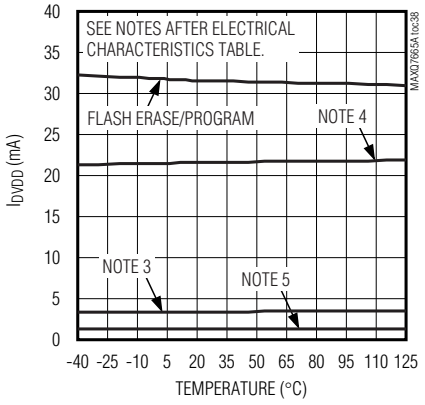
RC OSCILLATOR OUTPUT FREQUENCY vs. DV_{DD} SUPPLY VOLTAGE



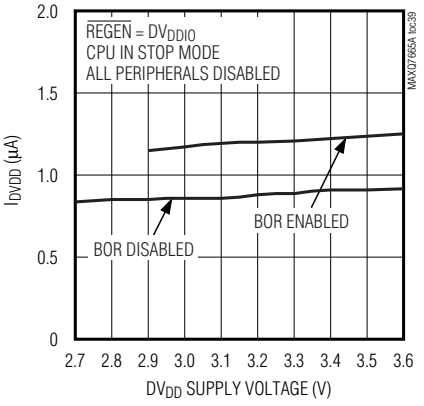
DV_{DD} ACTIVE SUPPLY CURRENT vs. DV_{DD} SUPPLY VOLTAGE



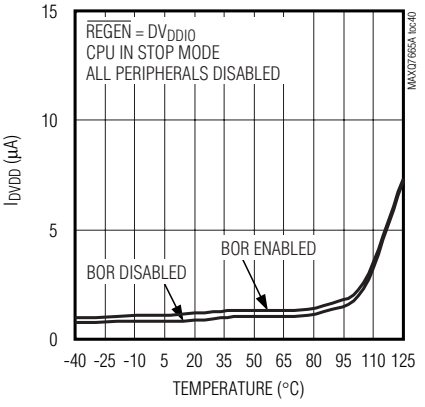
DV_{DD} ACTIVE SUPPLY CURRENT vs. TEMPERATURE



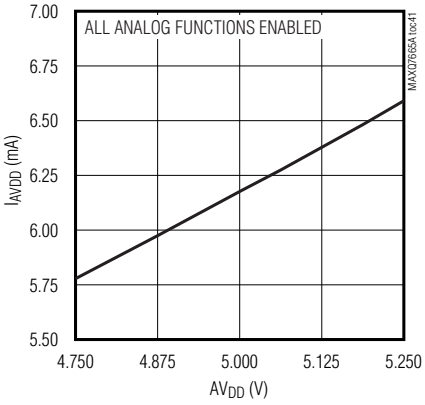
DV_{DD} STOP-MODE SUPPLY CURRENT vs. DV_{DD} SUPPLY VOLTAGE



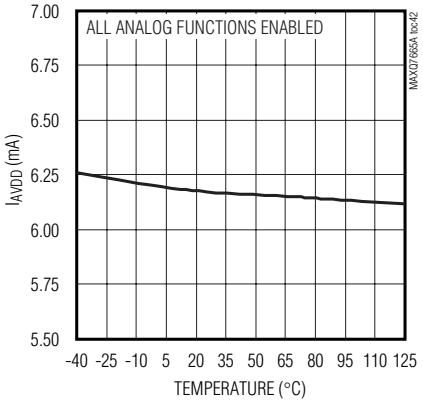
DV_{DD} STOP-MODE SUPPLY CURRENT vs. TEMPERATURE



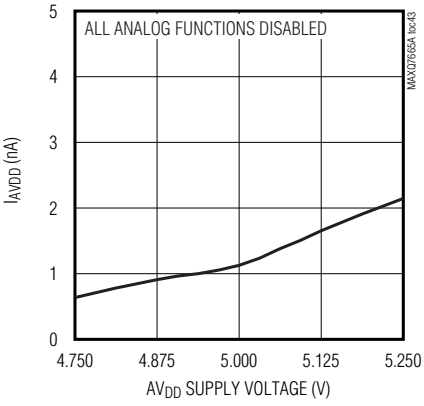
AV_{DD} ENABLED SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE



AV_{DD} ENABLED SUPPLY CURRENT vs. TEMPERATURE



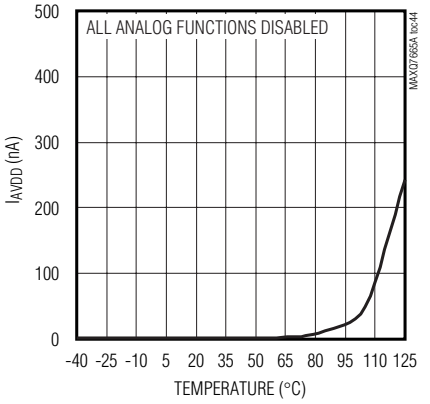
AV_{DD} DISABLED SUPPLY CURRENT vs. AV_{DD} SUPPLY VOLTAGE



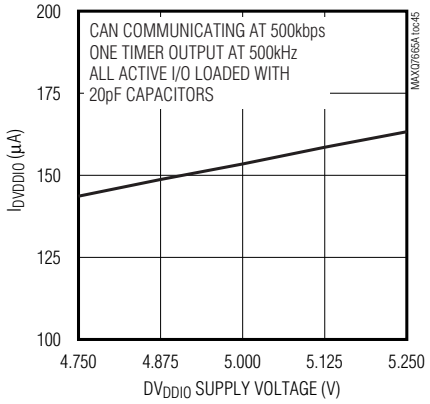
Typical Operating Characteristics (continued)

(AV_{DD} = DV_{DDIO} = +5.0V, DV_{DD} = +3.3V, f_{ADCCLK} = 8MHz, f_{ADC} = 500kHz, T_A = +25°C, unless otherwise noted.)

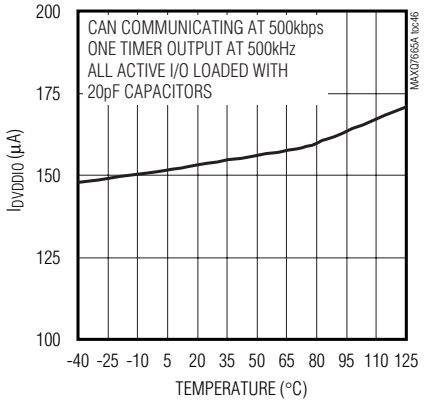
AV_{DD} DISABLED SUPPLY CURRENT vs. TEMPERATURE



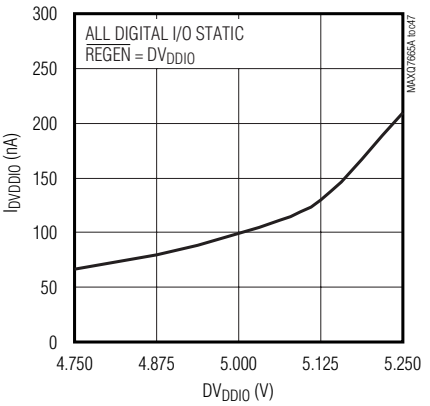
DV_{DDIO} DYNAMIC SUPPLY CURRENT vs. DV_{DDIO} SUPPLY VOLTAGE



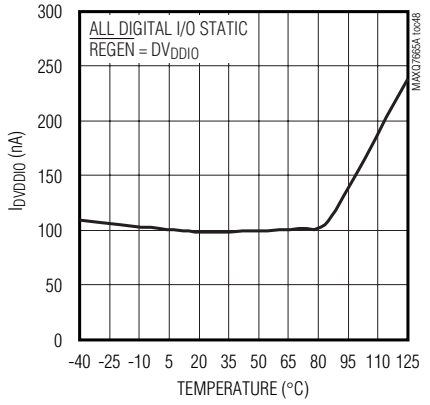
DV_{DDIO} DYNAMIC SUPPLY CURRENT vs. TEMPERATURE



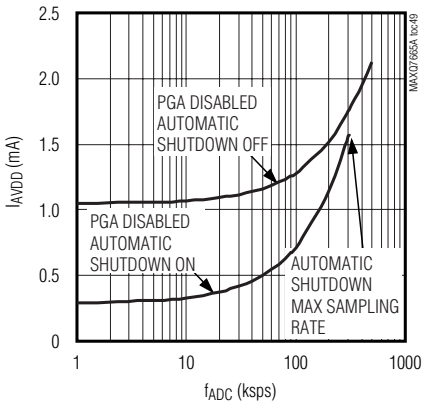
DV_{DDIO} STATIC SUPPLY CURRENT vs. DV_{DDIO} SUPPLY VOLTAGE



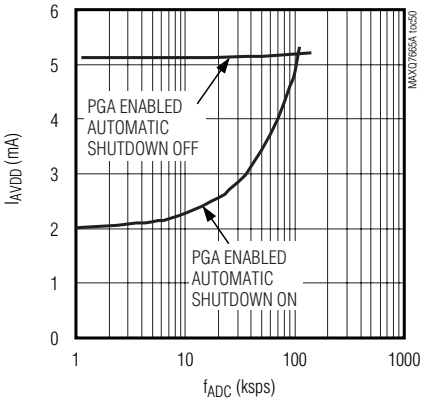
DV_{DDIO} STATIC SUPPLY CURRENT vs. TEMPERATURE



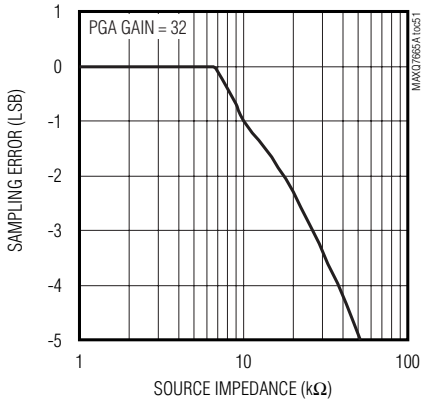
AV_{DD} SUPPLY CURRENT vs. ADC SAMPLING RATE



AV_{DD} SUPPLY CURRENT vs. ADC SAMPLING RATE (PGA ENABLED)



SAMPLING ERROR vs. INPUT SOURCE IMPEDANCE



16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Pin Description

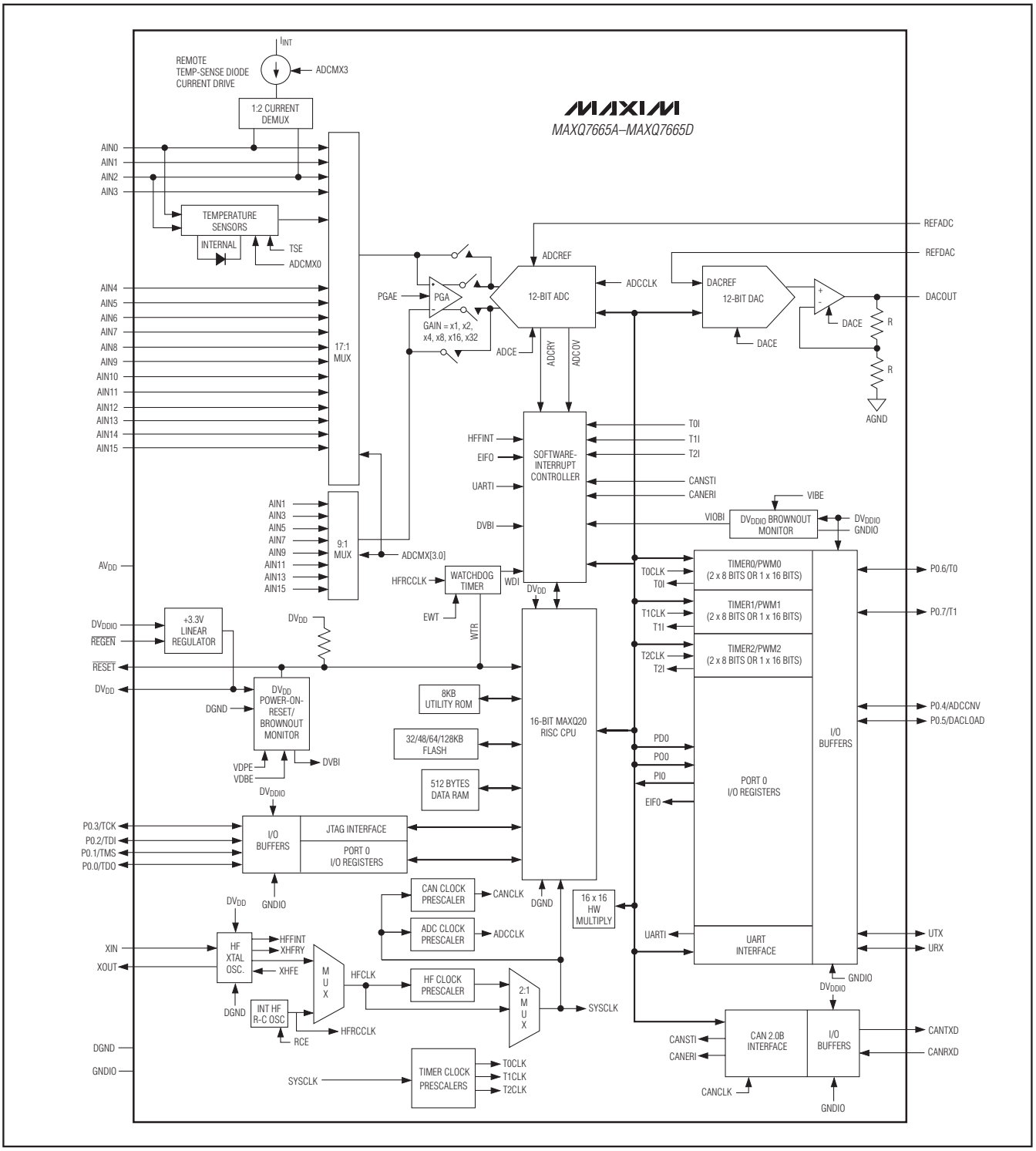
PIN	NAME	FUNCTION
1	AIN11	Analog Input Channel 11. AIN11 is multiplexed to the PGA as a differential input with AIN10.
2	AIN10	Analog Input Channel 10. AIN10 is multiplexed to the PGA as a differential input with AIN11.
3	AIN9	Analog Input Channel 9. AIN9 is multiplexed to the PGA as a differential input with AIN8.
4	AIN8	Analog Input Channel 8. AIN8 is multiplexed to the PGA as a differential input with AIN9.
5, 8	AGND	Analog Ground
6	REFADC	ADC External Reference Input. Connect an external reference voltage between 1V and AV_{DD} to REFADC.
7	REFDAC	DAC External Reference Input. Connect an external reference voltage between 0V and AV_{DD} to REFDAC.
9	AIN7	Analog Input Channel 7. AIN7 is multiplexed to the PGA as a differential input with AIN6.
10	AIN6	Analog Input Channel 6. AIN6 is multiplexed to the PGA as a differential input with AIN7.
11	AIN5	Analog Input Channel 5. AIN5 is multiplexed to the PGA as a differential input with AIN4.
12	AIN4	Analog Input Channel 4. AIN4 is multiplexed to the PGA as a differential input with AIN5.
13	AIN3	Analog Input Channel 3. AIN3 is multiplexed to the PGA as a differential input with AIN2. AIN3–AIN0 have remote temperature sensor capability.
14	AIN2	Analog Input Channel 2. AIN2 is multiplexed to the PGA as a differential input with AIN3. AIN3–AIN0 have remote temperature sensor capability.
15	AIN1	Analog Input Channel 1. AIN1 is multiplexed to the PGA as a differential input with AIN0. AIN3–AIN0 have remote temperature sensor capability.
16	AIN0	Analog Input Channel 0. AIN0 is multiplexed to the PGA as a differential input with AIN1. AIN3–AIN0 have remote temperature sensor capability.
17	DACOUT	DAC Buffer Output. DACOUT is the DAC voltage buffer output.
18, 19, 31	DGND	Digital Ground for the Digital Core and Flash
20	CANRXD	CAN Bus Receiver Input. Control area network receiver input.
21	CANTXD	CAN Bus Transmitter Output. Control area network transmitter output.
22	UTX	UART Transmitter Output
23	URX	UART Receiver Input
24	P0.6/T0	Port 0 Bit 6/Timer 0. P0.6 is a general-purpose digital I/O with interrupt/wake-up input capability. T0 is a primary timer/PWM input or output.
25	P0.7/T1	Port 0 Bit 7/Timer 1. P0.7 is a general-purpose digital I/O with interrupt/wake-up input capability. T1 is a primary timer/PWM input or output.
26, 39	DV_{DDIO}	Digital I/O Supply Voltage. Supplies all digital I/O except for XIN, XOUT, and $\overline{RESET}$. Bypass DV_{DDIO} to GNDIO with a 0.1µF capacitor placed as close as possible to the device. DV_{DDIO} is also connected to the input of the linear regulator.
27	GNDIO	Digital I/O Ground
28, 29	I.C.	Internal Connection. Connect I.C. to GNDIO or DV_{DDIO}.
30	N.C.	No Connection. No internal connection. Leave N.C. unconnected.
32	P0.0/TDO	Port 0 Data 0/JTAG Serial Test Data Output. P0.0 is a general-purpose digital I/O with interrupt/wake-up capability. TDO is the JTAG serial test, data output.

Pin Description (continued)

PIN	NAME	FUNCTION
33	P0.1/TMS	Port 0 Data 1/JTAG Test Mode Select. P0.1 is a general-purpose digital I/O with interrupt/wake-up capability. TMS is the JTAG test mode, select input.
34	P0.2/TDI	Port 0 Data 2/JTAG Serial Test Data Input. P0.2 is a general-purpose digital I/O with interrupt/wake-up capability. TDI is the JTAG serial test, data input.
35	P0.3/TCK	Port 0 Data 3/JTAG Serial Test Clock Input. P0.3 is a general-purpose digital I/O with interrupt/wake-up capability. TCK is the JTAG serial test, clock input.
36	P0.4/ADCCNV	Port 0 Data 4/ADC Start Conversion Control. P0.4 is a general-purpose digital I/O. ADCCNV is firmware configurable for a rising or falling edge start/convert to trigger ADC conversions.
37	P0.5/DACLOAD	Port 0 Data 5/DAC Data Register Load/Update Input. P0.5 is a general-purpose digital I/O with interrupt/wake-up capability. DACLOAD is firmware configurable for a rising or falling edge to update the DACOUT register.
38	$\overline{\text{REGEN}}$	Active-Low Linear Regulator Enable Input. Connect $\overline{\text{REGEN}}$ to GNDIO to enable the linear regulator. Connect to DV_{DDIO} to disable the linear regulator.
40	DV_{DD}	Digital Supply Voltage. DV_{DD} supplies the internal digital core and flash memory. DV_{DD} is internally connected to the output of the internal 3.3V linear regulator. Disable the internal regulator to connect DV_{DD} to an external supply. When using the on-chip linear regulator, bypass DV_{DD} to DGND with a 4.7µF ±20% capacitor with a maximum ESR of 0.5Ω. In addition, bypass DV_{DD} with a 0.1µF capacitor. Place both bypass capacitors as close as possible to the device.
41	$\overline{\text{RESET}}$	Reset Input and Output. Active-low open-drain input/output with internal 360kΩ pullup to DV_{DD}. Drive low to reset the µC. $\overline{\text{RESET}}$ is low during power-up reset and during DV_{DD} brownout conditions.
42	XOUT	High-Frequency Crystal Output. Connect an external crystal to XIN and XOUT for normal operation. Leave XOUT unconnected if XIN is driven with an external clock source. XOUT is not driven when using the internal RC oscillator.
43	XIN	High-Frequency Crystal Input. Connect an external crystal or resonator to XIN and XOUT for normal operation, or drive XIN with an external clock source. XIN is not driven when using the internal RC oscillator.
44	AV_{DD}	Analog Supply Voltage Input. Connect AV_{DD} to a +5V supply. Bypass AV_{DD} to AGND with a 0.1µF capacitor placed as close as possible to the device.
45	AIN15	Analog Input Channel 15. AIN15 is multiplexed to the PGA as a differential input with AIN14.
46	AIN14	Analog Input Channel 14. AIN14 is multiplexed to the PGA as a differential input with AIN15.
47	AIN13	Analog Input Channel 13. AIN13 is multiplexed to the PGA as a differential input with AIN12.
48	AIN12	Analog Input Channel 12. AIN12 is multiplexed to the PGA as a differential input with AIN13.
—	EP	Exposed Pad. EP is internally connected to AGND. Connect EP to AGND externally.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Block Diagram



Detailed Description

The µC arithmetic core of the MAXQ7665A–MAXQ7665D is a 16-bit RISC machine with digital and analog peripheral functions. They incorporate a 16-bit RISC ALU with a Harvard memory architecture that can address up to 128KB (64K x 16) of flash and 512 bytes (256 x 16) of RAM memory. They also contain a hardware multiplier, up to eight digital I/Os, a controller area network (CAN 2.0B) bus, a JTAG interface, three timers, an on-chip RC oscillator, a precision 12-bit 500ksps ADC with an 8-channel differential MUX and PGA, a 12-bit precision DAC, an internal temperature sensor and temperature-sensor driver, a linear regulator, watchdog timer, and a dual power-supply supervisor.

The MAXQ offers a low < 3mA/MIPS ratio. The on-chip 16-bit x 16-bit hardware multiplier with accumulator, performs single-cycle computations. Refer to the *MAXQ7665/MAXQ7666 User's Guide* for more detailed information on configuring and programming the MAXQ7665A–MAXQ7665D.

Analog Input Peripheral

The integrated 12-bit ADC employs an ultra-low-power, high-precision, SAR-based conversion method and can operate up to 500ksps (142ksps with PGA ≥ 2). The on-chip 8-channel differential MUX and PGA allow the ADC to measure eight fully differential analog inputs with software-selectable input ranges through the PGA. See Figure 1.

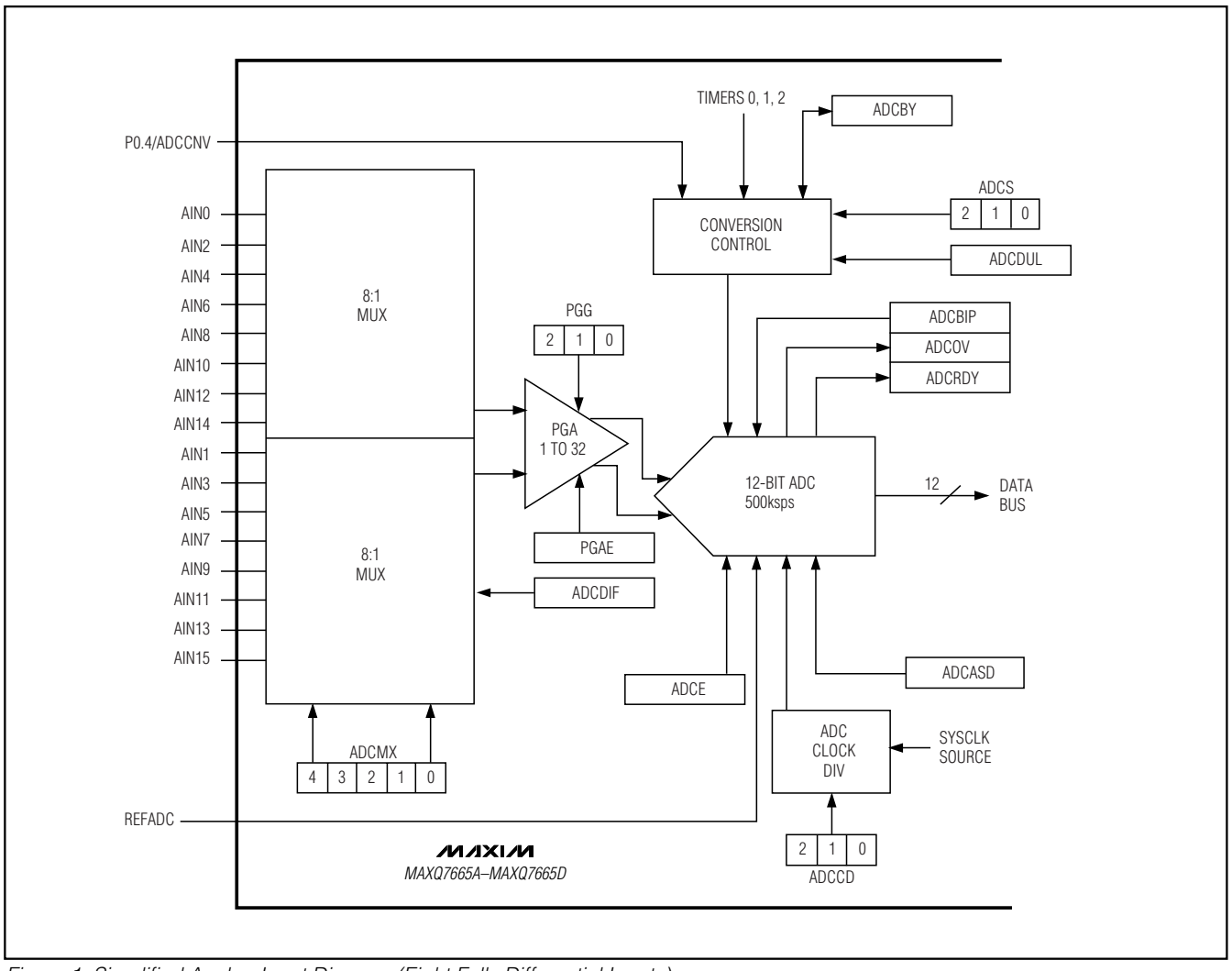


Figure 1. Simplified Analog Input Diagram (Eight Fully Differential Inputs)

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

The MAXQ7665A–MAXQ7665D ADC uses a fully differential SAR conversion technique and an on-chip T/H block to convert temperature and voltage signals into a 12-bit digital result. Differential configurations are supported using an analog input channel MUX that supports eight differential channels.

The differential analog inputs are selected from the following pairs: AIN0/AIN1, AIN2/AIN3, AIN4/AIN5, AIN6/AIN7, AIN8/AIN9, AIN10/AIN11, AIN12/AIN13, and AIN14/AIN15.

Remote temperature-sensor configuration in differential mode uses analog input channel pairs AIN2/AIN3 and AIN0/AIN1. In single-ended remote temperature-sensor configuration, only channels AIN2 and AIN0 are used. Internal temperature-sensor configuration measures local die temperature and does not use any analog input channel.

There are four ways to control the ADC conversion timing:

1) Software register bit control
2) Continuous conversion
3) Internal timers (T0, T1, or T2)
4) External input through pin ADCCNV

Refer to the *MAXQ7665/MAXQ7666 User's Guide* for more detailed information on the ADC and MUX.

12-Bit Digital-to-Analog Converter (DAC)

The MAXQ7665A–MAXQ7665D contain a 12-bit voltage-output DAC with its own output buffer. The data path to the DAC is double buffered and the output register can be updated using the DACLOAD digital input. Refer to the *MAXQ7665/MAXQ7666 User's Guide* for detailed programming information. The DAC also supports a square-wave-output toggle mode with precise amplitude control for applications that require pulse-amplitude modulation (PAM) and/or pulse-width modulation (PWM) signals. See Figure 2 for a simplified block diagram of the DAC.

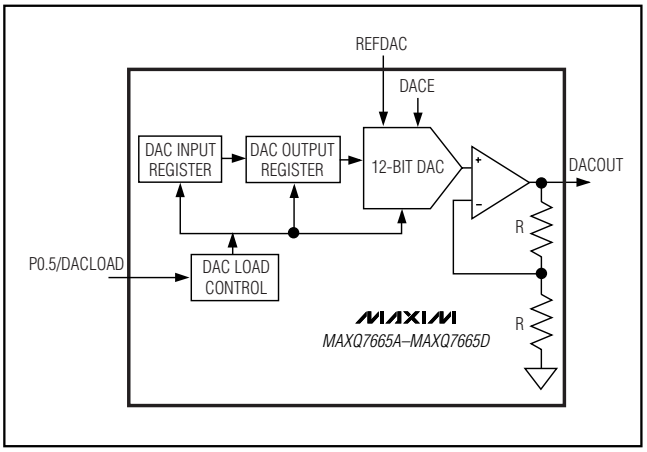


Figure 2. Simplified DAC Diagram

The DAC output buffer is in a voltage follower configuration (gain of 1V/V from REFDAC). The buffer can be disabled when not in use. When the buffer is disabled, the output is connected internally to AGND through a 100kΩ resistor. The reference input REFDAC accepts an input voltage of less than or equal to AV_{DD} for a maximum output swing of 0V to AV_{DD}.

Temperature Sensor

The µC measures temperature by using the on-chip ADC and a ROM-based tempConv subroutine. Use the tempConv subroutine to initiate a measurement (refer to the *MAXQ7665/MAXQ7666 User's Guide* for detailed information). The device supports conversions of two external and one on-chip (internal) temperature sensors. The external temperature sensor is typically a diode-connected small-signal transistor, connected between two analog inputs (differential) or one analog input and AGND (single-ended). Figures 3 and 4 illustrate these two configurations.

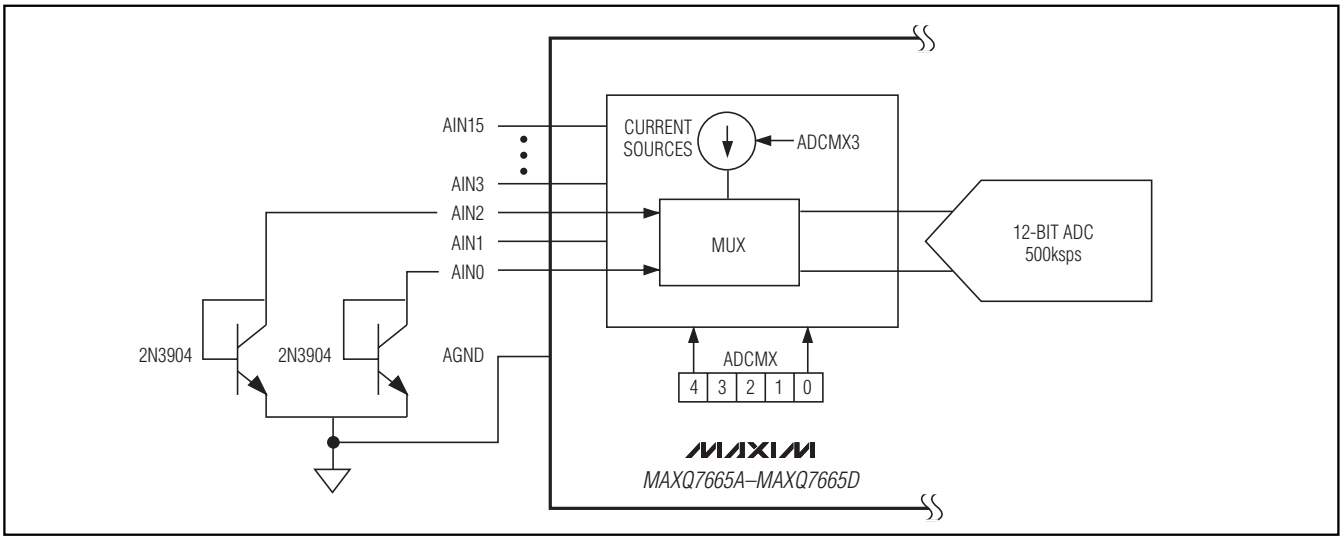


Figure 3. Temperature-Sensor Application Circuit—Single-Ended Configuration

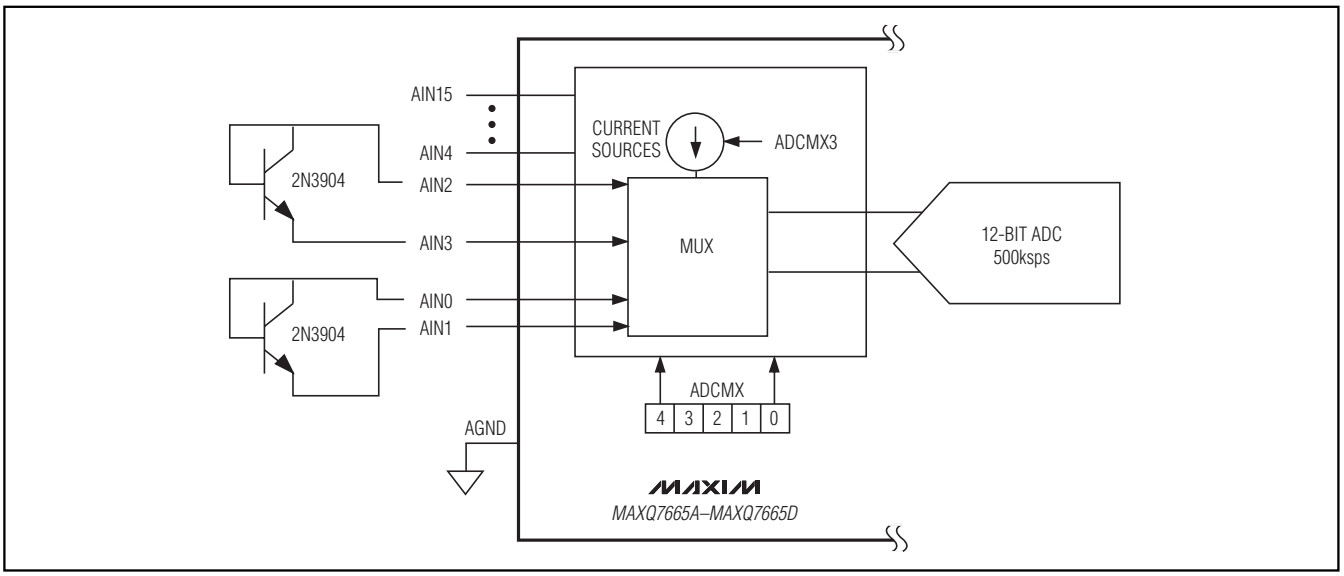


Figure 4. Temperature-Sensor Application Circuit—Differential Configuration

Power-On Reset and Brownout

Power supplies DV_{DD} and DV_{DDIO} each include a brownout monitor that alerts the µC through interrupt when their corresponding supply voltages drop below a selectable threshold. This condition is generally referred to as brownout interrupt (BOI), and these thresholds are set by the VDBI and VIOBI bits for DV_{DD} and DV_{DDIO}, respectively. Continuous monitoring ensures that a valid supply is present at all times while the µC is executing code. For example, the brownout monitors check that DV_{DDIO} does not drop during a CAN bus transfer, or DV_{DD} is not disrupted while the µC core is executing. The DV_{DDIO} brownout monitor also covers the analog peripherals if AV_{DD} and DV_{DDIO} are directly connected.

The DV_{DD} supply (internal core logic) also includes a voltage supervisor that controls the µC reset during power-up (DV_{DD} rising) and brownout (DV_{DD} falling) conditions (see Figure 5 for a POR and brownout timing example).

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

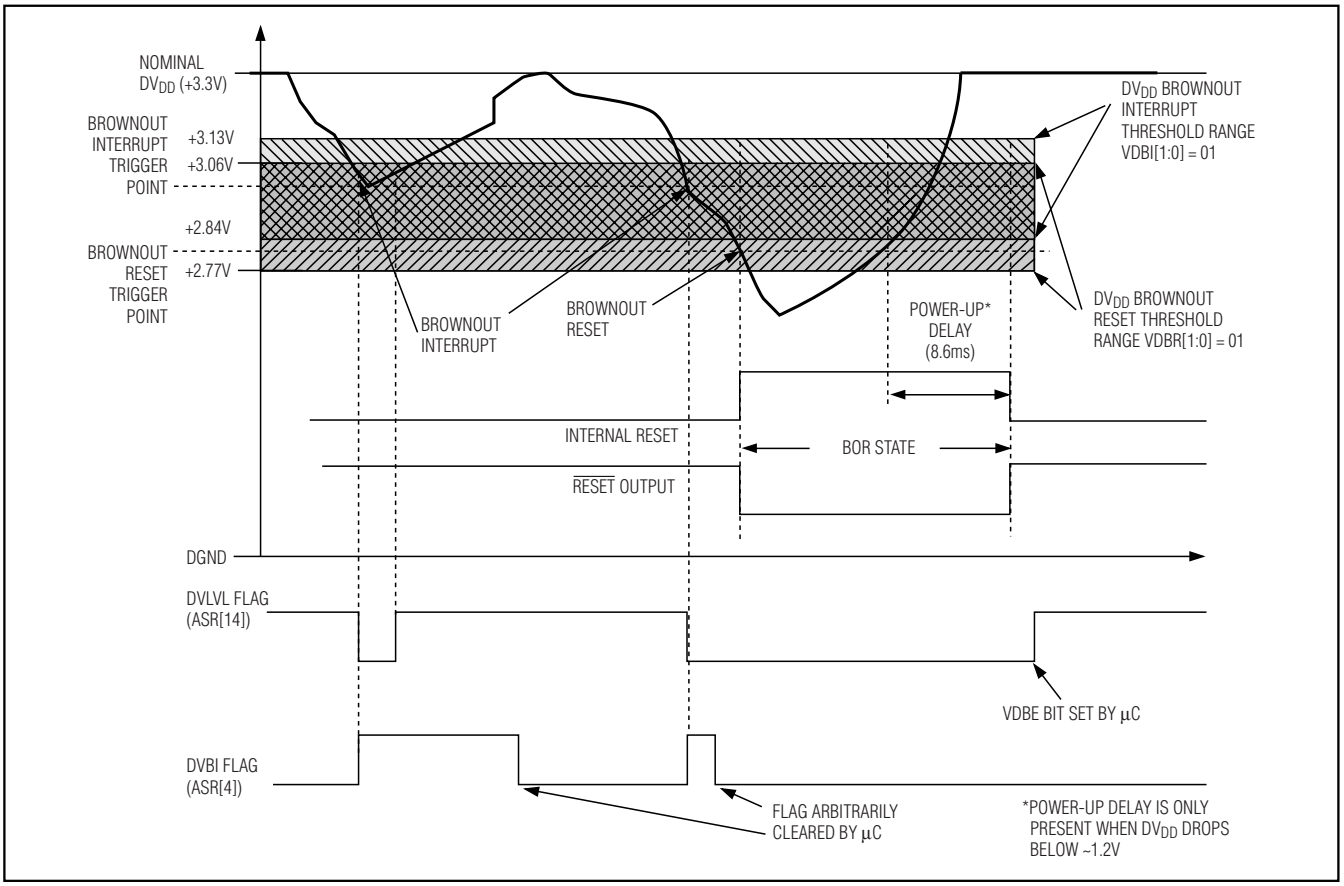


Figure 5. DV_{DD} Brownout Interrupt Detection

During power-up, $\overline{RESET}$ is held low once DV_{DD} rises above +1.0V. All internal register bits are set to their default, POR state after DV_{DD} exceeds a threshold of approximately +1.2V. This includes the VDBR bits which reset to 00b, resulting in a default, DV_{DD} brownout reset (BOR) threshold in the +2.7V to +2.99V range following POR. Once DV_{DD} rises above this DV_{DD} brownout threshold, the 7.6MHz RC oscillator starts driving the power-up counter, and 8.6ms (typ) later, the $\overline{RESET}$ pin is released and allowed to go high if nothing external is holding it low. An important system-design consideration at power-up is the DV_{DD} ramp-up rate should be at least 35mV/ms between +2.7V and +3.0V. This ensures $\overline{RESET}$ is not released before DV_{DD} reaches a minimum flash operating level of +3.0V. After DV_{DD} has reached a valid level and $\overline{RESET}$ is released, the µC jumps to the reset vector (8000h in the utility ROM), and the desired BOI and BOR threshold values can be set by the user through the VIOBI, VDBI, and VDBR bits.

If a valid DV_{DD} drops below its BOI threshold (set by the VDBI bits), an interrupt is generated. This offers the possibility of limited software cleanup before the DV_{DD} BOR occurs. The amount of cleanup time depends on the VDBI and VDBR brownout threshold bit settings, the size of the DV_{DD} bypass capacitors, and the application-dependent, µC power management and software cleanup tasks. Note that if the internal, +3.3V linear regulator is being used to provide DV_{DD}, additional software cleanup time is possible by using the DV_{DDIO} brownout monitor as an early warning that the regulator's DV_{DDIO} (+5V) input voltage is falling, and its DV_{DD} (+3.3V) will subsequently drop (unless DV_{DDIO} recovers).

As DV_{DD} continues to fall below the DV_{DD} BOR threshold set by the VDBR bits, the $\overline{RESET}$ pin is pulled low, µC and peripheral activity stops, and most, but not all of the register bits are set to their default state. This includes the VDBR bits, which retain their value if DV_{DD} falls below the BOR threshold, but not below the POR threshold.

Once DV_{DD} has entered BOR, there are a few possible scenarios:

- If DV_{DD} remains below the BOR threshold, the $\overline{RESET}$ pin remains low, and the µC remains in the reset state.
- If DV_{DD} stops falling before reaching the POR threshold, then begins rising above the BOR threshold, the $\overline{RESET}$ pin is released, and the µC jumps to the reset vector (8000h in the utility ROM). This is similar to the DV_{DD} power-up case described in the previous scenario, except there is no power-up counter delay and some of the register bits are set to BOR values rather than POR values. See Tables 3 and 5 for the reset behavior of specific bits. In particular, the retained VDBR setting, if higher than the default value of 00b, allows a potentially more robust brownout recovery closer to or above the minimum flash operating level of +3.0V.
- If DV_{DD} falls below the 1.2V POR threshold, all register bits are reset, and any DV_{DD} recovery from that point is identical to the power-up case described above. See Tables 3 and 5 for reset behavior of specific bits.

Refer to the *MAXQ7665/MAXQ7666 User's Guide* for detailed programming information, and a more thorough description of POR and brownout behavior.

Internal 3.3V Linear Regulator

The MAXQ7665A–MAXQ7665D core logic supply, DV_{DD}, can be supplied by a 3.3V external supply or the on-chip 3.3V, 50mA linear regulator. To use the on-chip linear regulator, ensure the DV_{DDIO} supply can support a load of approximately 50mA and connect digital input $\overline{REGEN}$ to GNDIO. If using an external supply, connect the regulated 3.3V supply to DV_{DD} and connect digital input $\overline{REGEN}$ to DV_{DDIO}. If the linear regulator is not used, bring up DV_{DDIO} before DV_{DD}.

System Clock Generator

The MAXQ7665A–MAXQ7665D oscillator module is the master clock generator that supplies the system clock for the µC core and all of the peripheral modules. The high-frequency (HF) oscillator is designed to operate with a 1MHz to 8MHz crystal. Alternatively, the on-chip RC oscillator can be used in applications that do not require precise timing. Due to its RISC design, the MAXQ7665A–MAXQ7665D execute most instructions in a single SYSCLK period. The oscillator module contains all of the primary clock-generation circuitry. Figure 6 shows a block diagram of the system clock module.

The MAXQ7665A–MAXQ7665D contain many features for generating a master clock signal timing source:

- Internal, fast-starting, 7.6MHz RC oscillator eliminates external crystal
- Internal high-frequency oscillator that can drive an external 1MHz to 8MHz crystal
- External high-frequency clock input (up to 8MHz)
- Selectable internal capacitors for HF crystal oscillator
- Power-up timer
- Power-saving management modes
- Fail-safe modes

Watchdog Timer

The watchdog timer serves as a time-base generator, an event timer, or a system supervisor. The primary function of the watchdog timer is to supervise software execution, watching for stalled or stuck software. The watchdog timer performs a controlled system restart when the µP fails to write to the watchdog timer register before a selectable timeout interval expires. In some designs, the watchdog timer is also used to implement a real-time operating system (RTOS) in the µC. When used to implement an RTOS, a watchdog timer typically has four objectives:

1) To detect if a system is operating normally
2) To detect an infinite loop in any of the tasks
3) To detect an arbitration deadlock involving two or more tasks
4) To detect if some lower priority tasks are not getting to run because of higher priority tasks

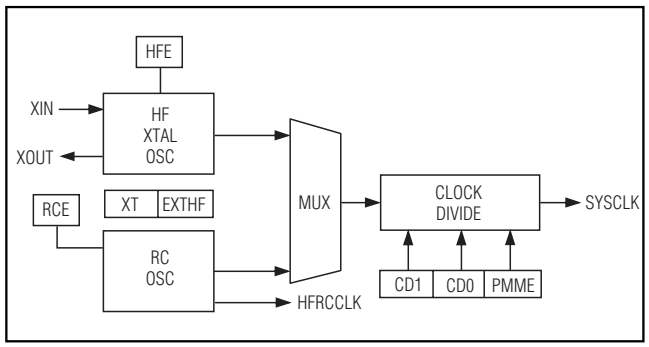


Figure 6. High-Frequency and RC Oscillator Block Diagram

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

As illustrated in Figure 7, the high-frequency internal RC oscillator (HFRCCLK) drives the watchdog timer through a series of dividers. The divider output is programmable and determines the timeout interval. When enabled, the interrupt flag WDIF is set when a timeout is reached. A system reset then occurs after a time delay (based on the divider ratio).

The watchdog timer functions as the source of both the watchdog interrupt and the watchdog reset. The interrupt timeout has a default divide ratio of 2^{12} of the HFRCCLK, with the watchdog reset set to timeout 2^9 clock cycles later. With the nominal RC oscillator value of 7.6MHz, an interrupt timeout occurs every 539µs, followed by a watchdog reset 67.4µs later. The watchdog timer is reset to the default divide ratio following any reset. Using the WD0 and WD1 bits in the WDCN register, other divide ratios can be selected for longer watchdog interrupt periods. If the WD[1:0] bits are changed before the watchdog interrupt timeout occurs (i.e. before the watchdog reset counter begins), the watchdog timer count is reset. All watchdog timer reset timeouts follow the programmed interrupt timeout 512 source clock cycles later. For more information on the MAXQ7665A–MAXQ7665D watchdog timer, refer to the *MAXQ7665/MAXQ7666 User's Guide.*

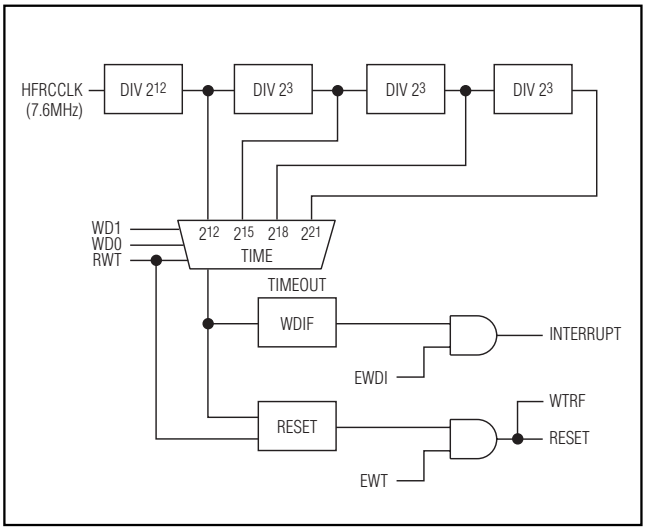


Figure 7. Watchdog Functional Diagram

Timer and PWM

The MAXQ7665A–MAXQ7665D include three 16-bit timer channels. Each timer is a type 2 timer implemented in the MAXQ family (see Figure 8). Two of the timers are accessible through I/Os, and one is accessible only through software. Type 2 timers are auto-reload 16-bit timers/counters offering the following functions:

- 8-bit/16-bit timer/counter
- Up/down auto-reload
- Counter function of external pulse
- Capture
- Compare

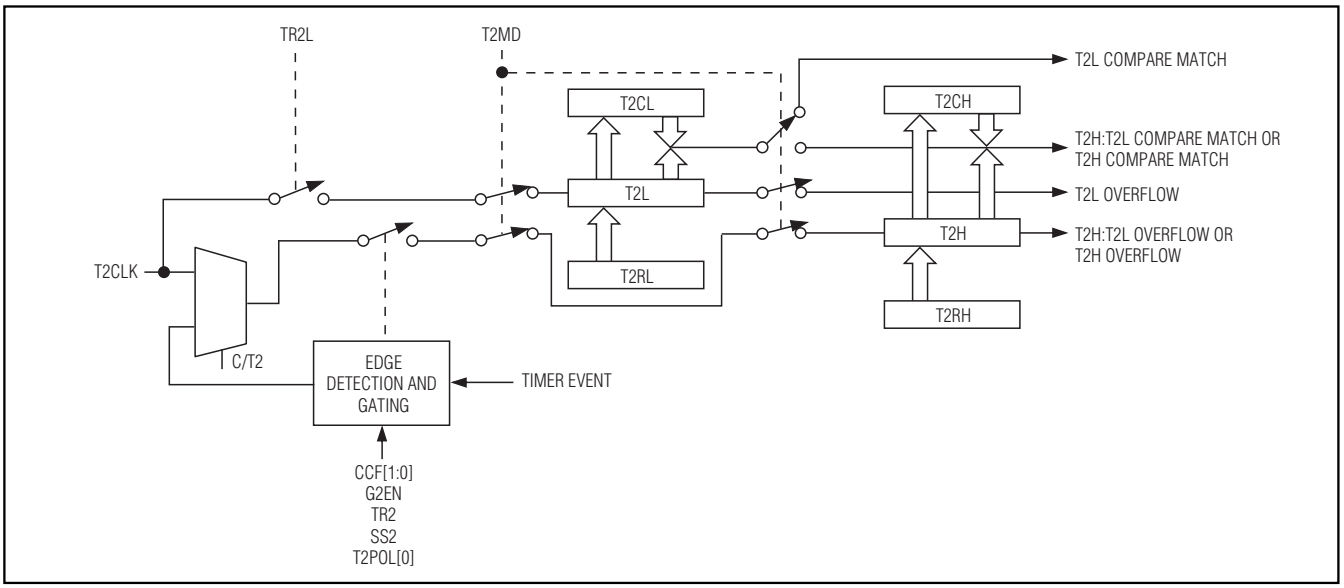


Figure 8. Type 2 Timer Functional Diagram

Note: The MAXQ7665A–MAXQ7665D do not have secondary timer I/O pins (such as T0B and T1B) that are present in some other MAXQ products.

16-Bit x 16-Bit Hardware Multiplier

A hardware multiplier supports high-speed multiplications. The multiplier is capable of completing a 16-bit x 16-bit multiply in a single cycle and contains a 48-bit accumulator that requires one more cycle. The multiplier is not part of the MAXQ core function but a peripheral that performs seven different multiply operations without interfering with the normal core functions:

- Unsigned 16-bit multiplication (one cycle)
- Unsigned 16-bit multiplication and accumulation (two cycles)
- Unsigned 16-bit multiplication and subtraction (two cycles)
- Signed 16-bit multiplication (one cycle)
- Signed 16-bit multiplication and negate (one cycle)
- Signed 16-bit multiplication and accumulation (two cycles)
- Signed 16-bit multiplication and subtraction (two cycles)

Figure 9 illustrates the simplified hardware multiplier circuitry. Two 16-bit parallel-load registers and a 48-bit accumulator are used: operand A (MA), operand B (MB), and accumulator (MC). The accumulator is formed by three 16-bit parallel registers (MC2, MC1, and MC0). The overflow bit is organized in the MCNT status/control register. The multiplicand and the multiplier are initially loaded into the MA and MB registers, respectively. Loading the required operands triggers the respective multiply, multiply-accumulate/subtract or multiply-negate operation. The multiply operation completes in a single cycle with the results in the read-only MC1R/MC0R register. The multiply-accumulate/subtract operation requires one extra wait cycle for the results to be stable in the MC2, MC1, and MC0 registers.

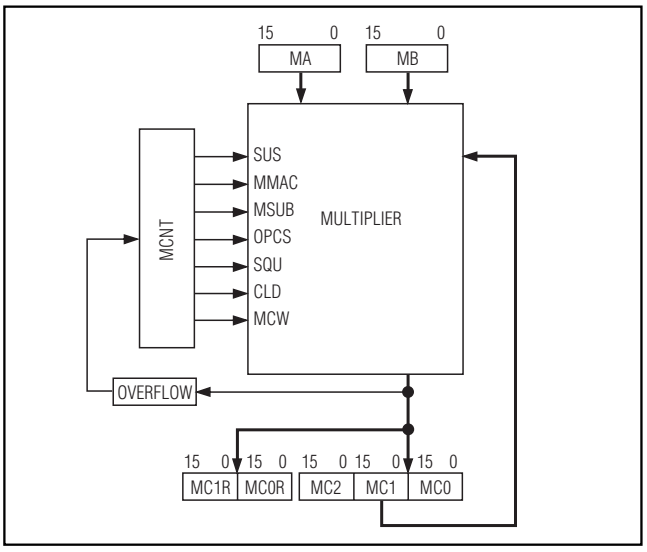


Figure 9. 16-Bit Hardware Multiplier Functional Diagram

The main arithmetic unit is the 16-bit x 16-bit multiplier, which processes operands feeding from the MA and MB registers and generates a 32-bit final product. The product value goes through the 32-bit adder to perform final accumulation with zeroes for multiply operation or with the contents from the MC1 and MC0 registers for multiply-accumulation. The final sum is accessible directly from the accumulator.

To support negate operations including signed multiply-negate and signed and unsigned multiply-subtract, the operand in MA is negated by 1's complement operation before being supplied to the arithmetic unit and the partial product terms are sign corrected. Refer to the *MAXQ7665/MAXQ7666 User's Guide* for more detailed information.

CAN Interface Bus

The MAXQ7665A–MAXQ7665D incorporate a CAN controller that is fully compliant with the CAN 2.0B specification.

The µC interface to the CAN controller is broken into two groups of registers. To simplify the software associated with the operation of the CAN controllers, most of the global CAN status and controls as well as the individual message center control/status registers are located in the peripheral register map. The remaining registers associated with the data identification, identification masks, format, and data are located in a dual port memory to allow the CAN controller and the processor access to the required functions. The CAN controller can directly access the dual port memory. A dedicated interface is incorporated to support dual port memory accessing by the processor through the CAN 0 data pointer (C0DP) and the CAN 0 data buffer (C0DB) special function registers.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

CAN Functional Description

The basic functions covered by the CAN controller include the use of 11-bit standard or 29-bit extended acceptance identifiers, as programmed by the µC for each message center, as shown in Figure 10. The CAN unit provides storage for up to 15 messages, with the standard 8-byte data field, in each message.

Each of the first 14 message centers is programmable in either transmit or receive mode. Message center 15 is designed as a receive-only message center with a buffer FIFO arrangement to help prevent the inadvertent loss of data when the µC is busy and is not allowed time to retrieve the incoming message prior to the acceptance of a second message into message center 15. Message center 15 also utilizes an independent set of mask registers and identification registers, which are only applied once an incoming message has not been accepted by any of the first 14 message centers. A second filter test is also supported for all message centers (1–15) to allow the CAN controller to use two separate 8-bit media masks and media arbitration fields to verify the contents of the first 2 bytes of data of

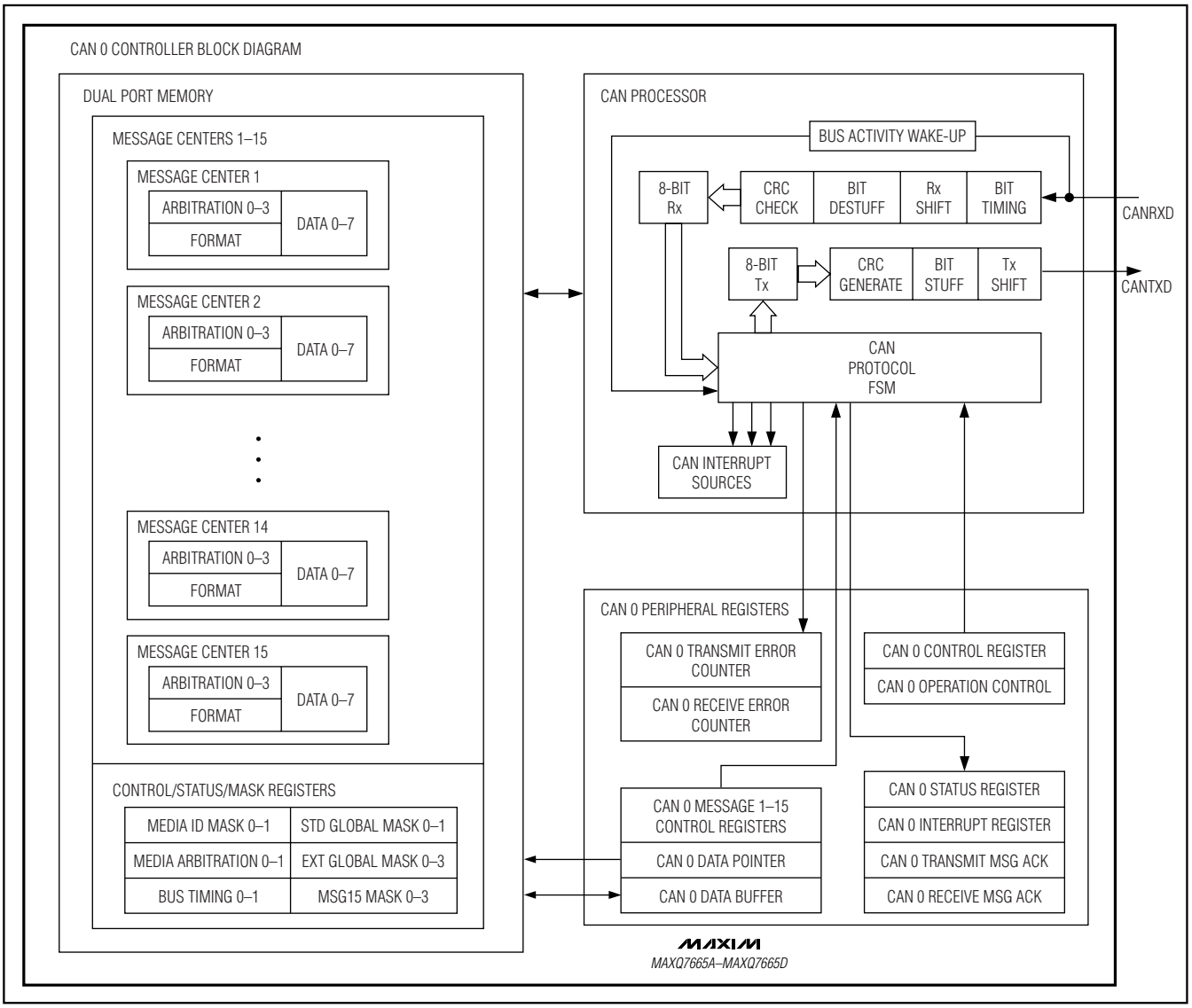


Figure 10. CAN 0 Controller Block Diagram

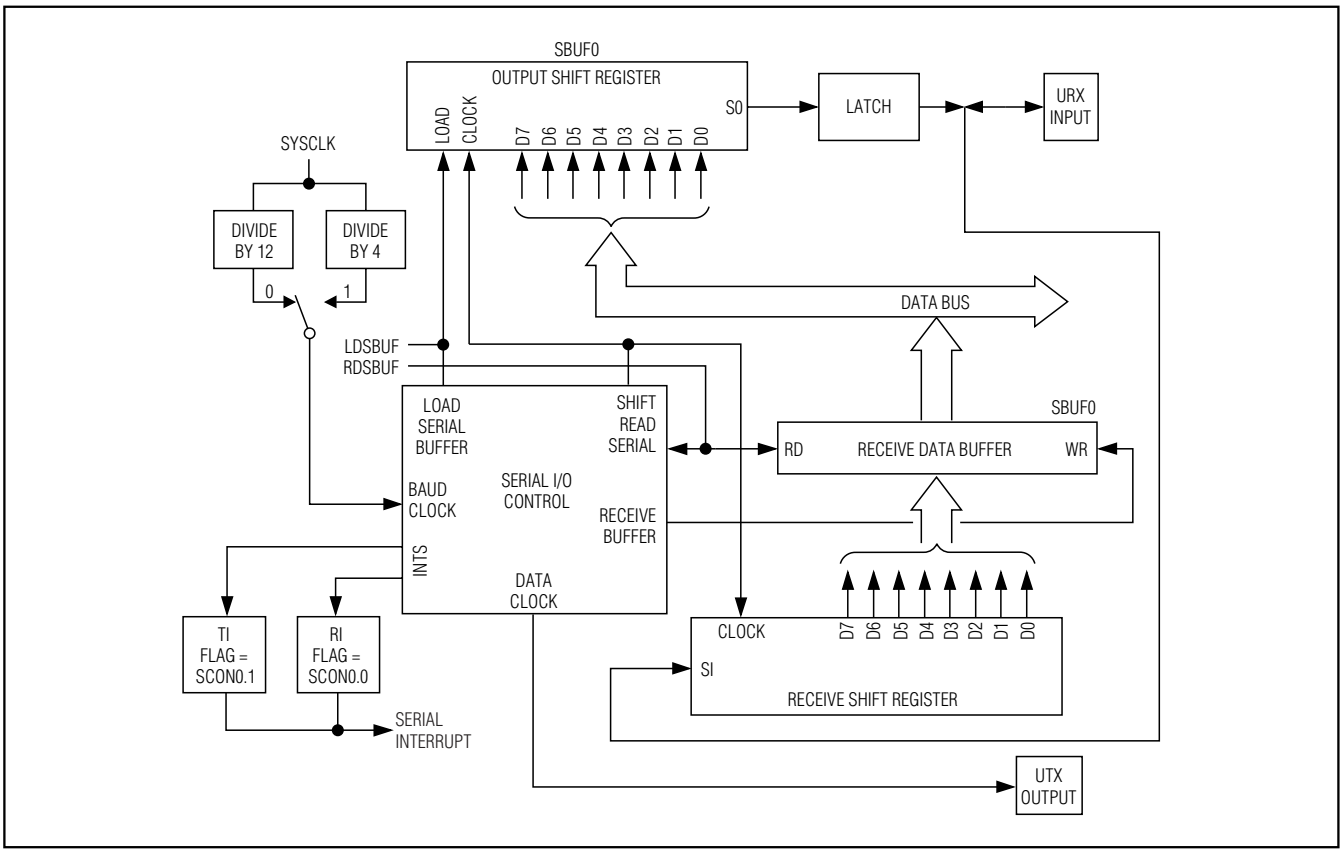


Figure 11a. UART Synchronous Mode (Mode 0)

each incoming message, before accepting an incoming message. This feature allows the CAN unit to directly support the use of higher CAN protocols, which make use of the first and/or second byte of data as a part of the acceptance layer for storing incoming messages. Each message center can also be programmed independently to perform testing of the incoming data with or without the use of the global masks.

Global controls and status registers in the CAN unit allow the µC to evaluate error messages, validate new data and the location of such data, establish the bus timing for the CAN bus, establish the identification mask bits, and verify the source of individual messages. In addition, each message center is individually equipped with the necessary status and controls to establish directions, interrupt generation, identification mode (standard or extended), data field size, data status, automatic remote frame request and acknowledgment, and masked or nonmasked identification acceptance testing.

UART Interface

Serial interfacing is provided through one (UTX/URX) 8051-style universal synchronous/asynchronous receiver/transmitter (UART) capable of interfacing with a LIN transceiver. Figure 11a shows the UART block diagram in synchronous mode and Figure 11b shows asynchronous mode. The UART allows the device to conveniently communicate with other RS-232 interface-enabled devices, as well as PCs and serial modems when paired with an external RS-232 line driver/receiver. The UART can detect framing errors and indicate the condition through a user-accessible software bit. The time base of the serial port is derived from either a division of the system clock or the dedicated baud clock generator. The UART is capable of supporting LIN protocol implementation in software when using one of the timers for autobaud

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

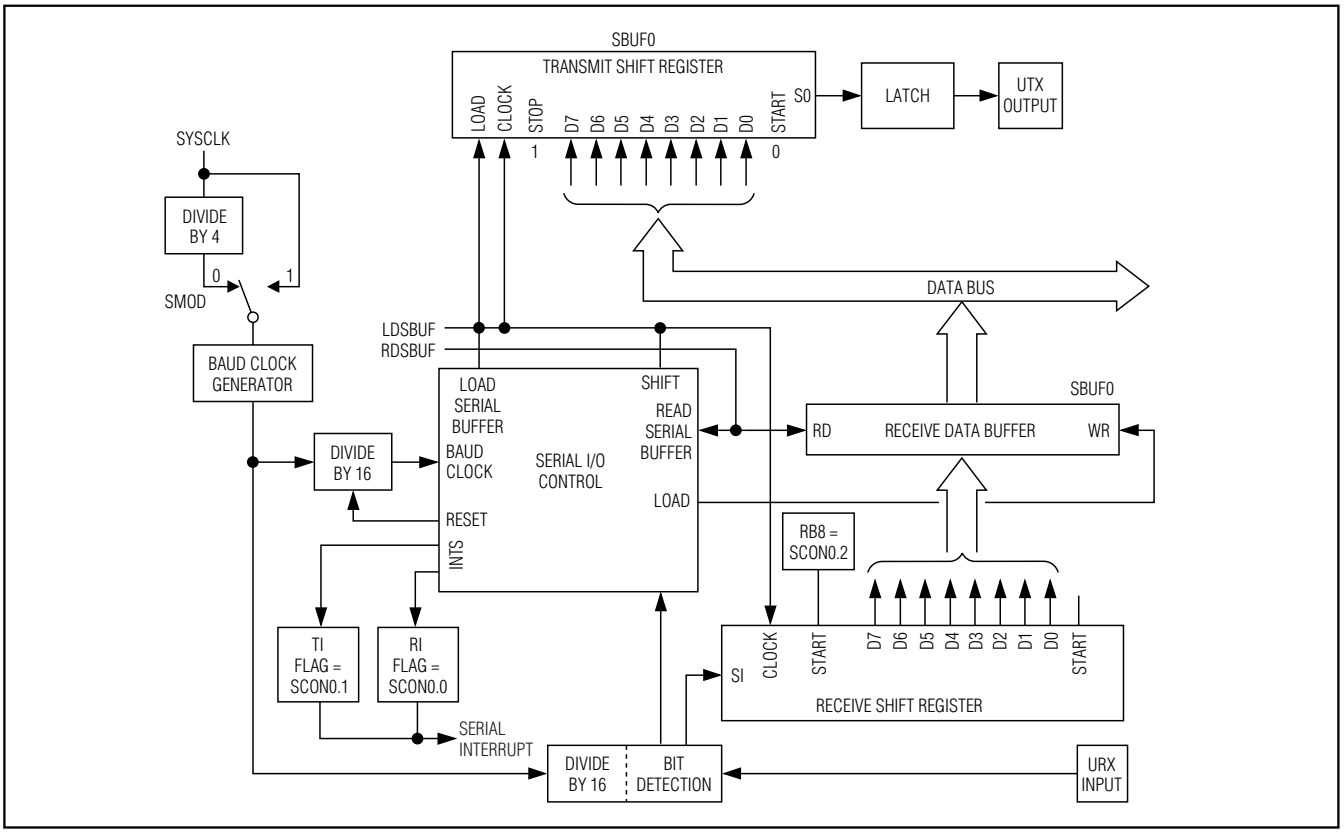


Figure 11b. UART Asynchronous Mode (Mode 1)

detection. Table 1 summarizes the operating characteristics as well as the maximum baud rate of each mode.

JTAG Interface Bus

The joint test action group (JTAG) IEEE 1149.1 standard defines a unique method for in-circuit testing and programming. The MAXQ7665A–MAXQ7665D conform to this standard, implementing an external test access port (TAP) and internal TAP controller for communication with a JTAG bus master, such as an automatic test equipment (ATE) system. For detailed information on the TAP and TAP controller, refer to *IEEE Standard 1149.1* on the IEEE website at http://standards.ieee.org. The JTAG on the MAXQ7665A–MAXQ7665D is used for in-circuit emulation and debug support, but does not support boundary scan test capability.

The TAP controller communicates synchronously with the host system (bus master) through four digital I/O pins: test mode select (TMS), test clock (TCK), test data input (TDI), and test data output (TDO). The internal TAP module consists of several shift registers and a

Table 1. Operating Characteristics and Mode Baud Rate

MODE	TYPE	BAUD CLOCK	START BITS	DATA BITS	STOP BITS	MAX BAUD RATE AT 8MHz
Mode 0	Synchronous	4 or 12 clock	N/A	8	N/A	2Mbps
Mode 1	Asynchronous	Baud generation	1	8	1	250kbps
Mode 2	Asynchronous	32 or 64 clock	1	8 + 1	1	250kbps
Mode 3	Asynchronous	Baud generation	1	8 + 1	1	250kbps

TAP controller (see Figure 12). The shift registers serve as transmit-and-receive data buffers for a debugger. From a JTAG perspective, shift registers are user-defined optional data registers. The bypass register and the instruction register, for example, are realized as a set of shift-register-based elements connected in parallel between a common serial input (TDI) and a common serial output (TDO). The instruction register, through the TAP controller, selects one of the registers to form an active serial path.

The maximum TCK clock frequency must be below 1/8 of the system clock frequency to work properly. The TAP operates asynchronously with on-chip system logic and may be affected by the timing relationship between the on-chip state machines and the TAP. The on-chip state machines are clocked by the system clock.

The four digital I/Os that form the TAP module are described as follows:

- TDO—Serial output signal for test instruction and data. Data is driven out only on the falling edge of TCK and is forced in an inactive state when it is idle. This signal is used to serially transfer internal data to the host. Data is transferred LSB first.
- TDI—Serial input signal for test instruction and data. Data should be driven in only on the rising edge of TCK. This signal is used to serially transfer data from

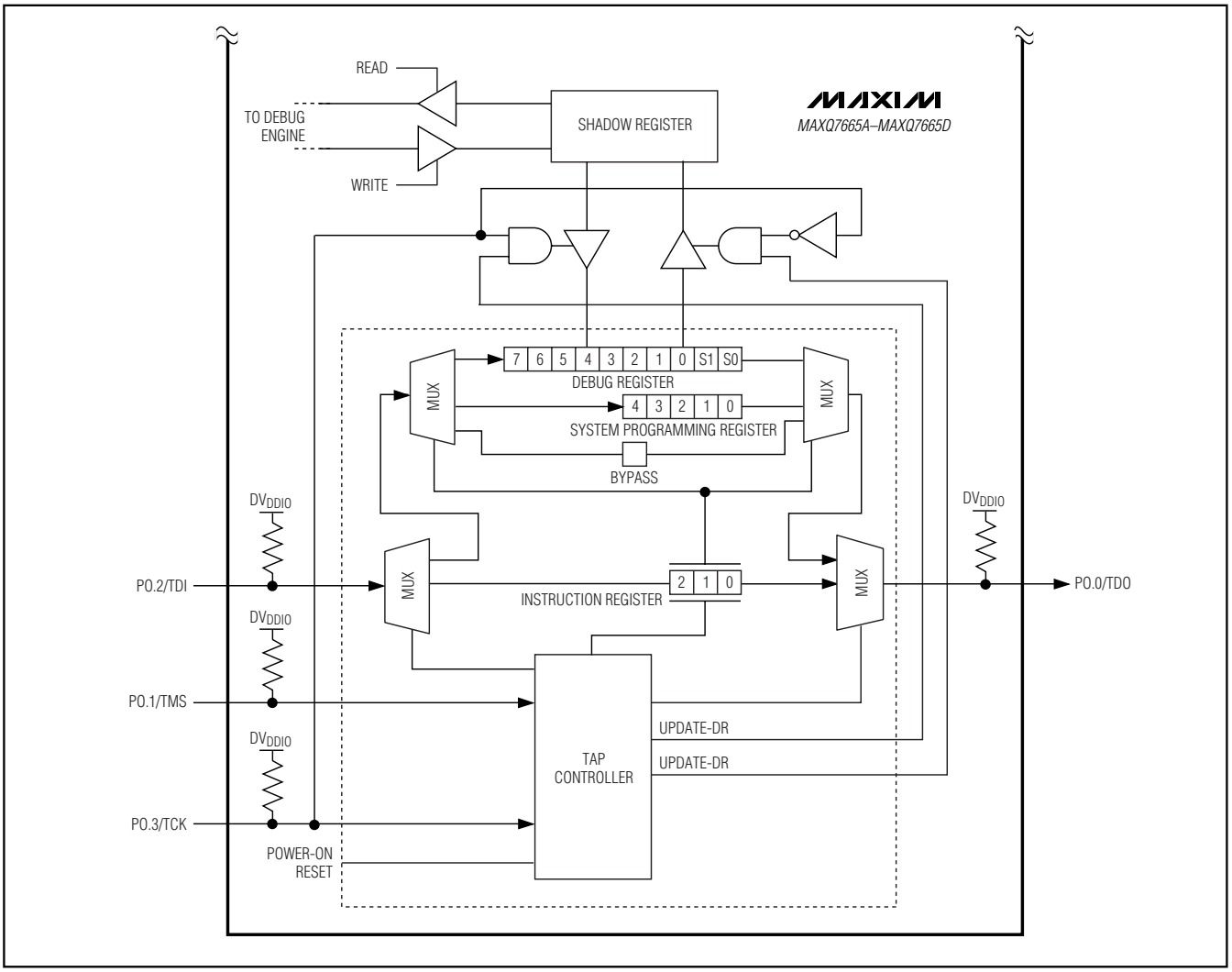


Figure 12. JTAG Interface Block Diagram

the host to the internal TAP module shift registers. Data is transferred LSB first.

- TCK—Serial clock for the test logic.
- TMS—Test mode selection. Test signals received at TMS are sampled at the rising edge of TCK and decoded by the TAP controller to control the test operation.

General-Purpose Digital I/Os

The MAXQ7665A–MAXQ7665D provide eight general-purpose digital I/Os (GPIOs). All GPIOs have an additional special function (SF), such as a timer input/output, or TAP signal for JTAG communication. For example, the state of pin P0.6/T0 can be programmed to depend on timer channel 0 logic. When programmed as a port, each I/O is configurable for high-impedance or weak pullup to DV_{DDIO}. At power-up, each GPIO is configured as an input with pullups to DV_{DDIO}. Note that at power-up, the JTAG function is enabled and should be turned off before normal operation. In addition, each GPIO can be programmed to cause an interrupt (on falling or rising edges). In stop mode, any interrupt can be used to wake up the device.

The data input/output direction in a port is independently controlled by the port direction register (PD). Each I/O within the port can be individually set as an output or input. The port output register (PO) contains the current state of the logic output buffers. When an I/O is configured as an output, writing to the PO register controls the output logic state. Reading the PO register shows the current state of the output buffers, independent of the data direction. The port input register (PI) is a read-only register that always reflects the logic state of the I/Os. When an I/O is configured as an input, writing to the PO register enables/disables the pull-up resistor. Refer to the *MAXQ7665/MAXQ7666 User's Guide* for more detailed information.

Port Characteristics

The MAXQ7665A–MAXQ7665D contain only one port (P0). It is a bidirectional 8-bit I/O port, which contains the following features:

- Schmitt trigger input circuitry with software-selectable high-impedance or weak pullup to DV_{DDIO}
- Software-selectable push-pull CMOS output drivers capable of sinking and sourcing 1.6mA
- Software-selectable open-drain output drivers capable of sinking 1.6mA
- Falling or rising edge interrupt capability
- All I/Os contain an additional special function, such as a logic input/output for a timer channel. Selecting an I/O for a special function alters the port characteristics of that I/O (refer to the *MAXQ7665/MAXQ7666 User's Guide* for more details). Figure 13 illustrates the functional blocks of an I/O.

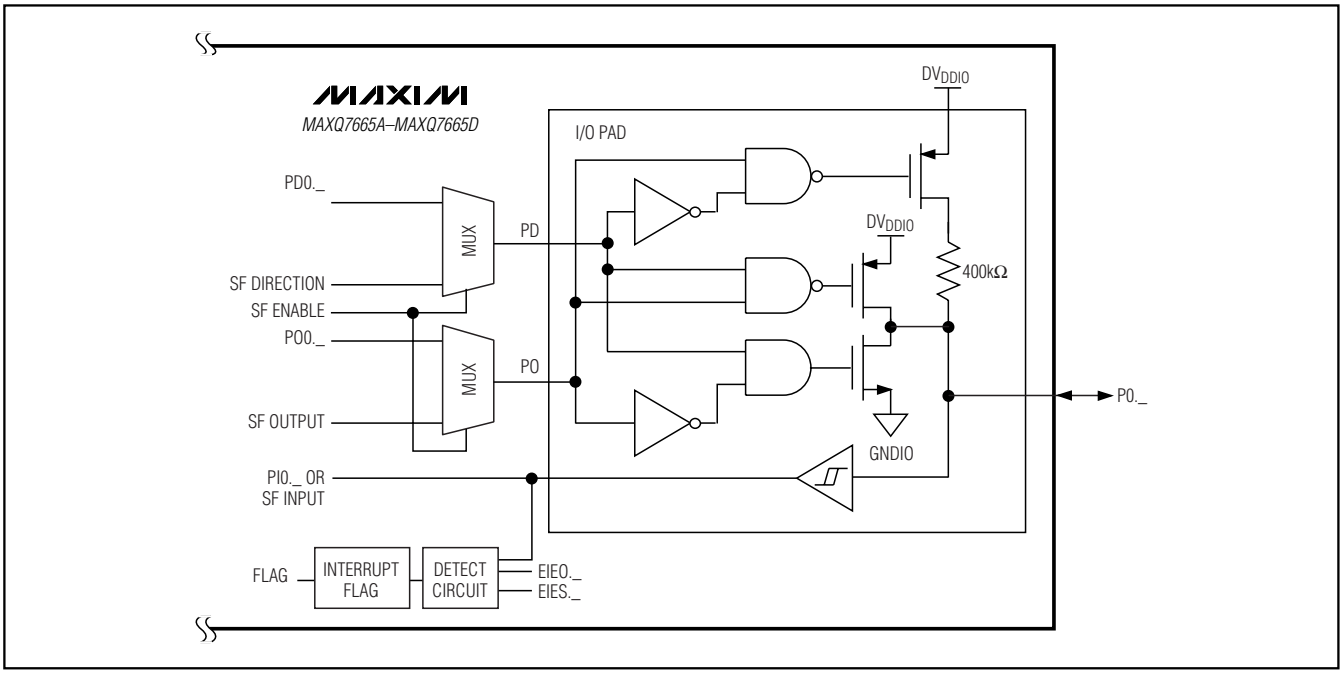


Figure 13. Digital I/O Circuitry

MAXQ Core Architecture

The MAXQ7665A–MAXQ7665D are low-cost, high-performance, CMOS, fully static, 16-bit µCs with flash memory and are members of the MAXQ family of µCs. The MAXQ7665A–MAXQ7665D are structured on a highly advanced, accumulator-based, 16-bit RISC architecture. Fetch and execution operations are completed in one cycle without pipelining, because the instruction contains both the operation code and data. The result is a streamlined 8 million instructions-per-second (MIPS) µC.

The highly efficient core is supported by a 16-level hardware stack, enabling fast subroutine calling and task switching. Data can be quickly and efficiently manipulated with three internal data pointers. Multiple data pointers allow more than one function to access data memory without having to save and restore data pointers each time. The data pointers can automatically increment or decrement following an operation, eliminating the need for software intervention. As a result, application speed is greatly increased.

Instruction Set

The instruction set is composed of fixed-length, 16-bit instructions that operate on registers and memory locations. The instruction set is highly orthogonal, allowing arithmetic and logical operations to use any register along with the accumulator. Special-function registers (also called peripheral registers) control the peripherals and are subdivided into register modules. The family architecture is modular, so that new devices and modules can reuse code developed for existing products.

The architecture is transport-triggered. This means that writes or reads from certain register locations can also cause side effects to occur. These side effects form the basis for the higher level operation codes defined by the assembler, such as ADDC, OR, JUMP, etc. The operation codes are actually implemented as MOVE instructions between certain register locations, while the assembler handles the encoding, which need not be a concern to the programmer.

The 16-bit instruction word is designed for efficient execution. Bit 15 indicates the format for the source field of the instruction. Bits 0 to 7 of the instruction represent the source for the transfer. Depending on the value of the format field, this can either be an immediate value or a source register. If this field represents a register, the lower 4 bits contain the module specifier and the upper 4 bits contain the register index in that module.

Bits 8 to 14 represent the destination for the transfer. This value always represents a destination register, with the lower 4 bits containing the module specifier and the upper 3 bits containing the register subindex within that module. Any time that it is necessary to directly select one of the upper 24 registers as a destination, the prefix register, PFX, is needed to supply the extra destination bits. This prefix register write is inserted automatically by the assembler and requires only one additional execution cycle.

Memory Organization

The MAXQ7665A–MAXQ7665D incorporate several memory areas:

- 8KB (4K x 16) utility ROM
- Up to 128KB (64K x 16) of flash memory for program storage
- 512 bytes (256 x 16) of SRAM for storage of temporary variables
- 16-level stack memory for storage of program return addresses and general-purpose use

The memory is arranged by default in a Harvard architecture, with separate address spaces for program and data memory (see Figure 14). A special mode allows data memory to be mapped into program space, permitting code execution from data memory. In addition, another mode allows program memory to be mapped into data space, permitting code constants to be accessed as data memory.

The incorporation of flash memory allows the devices to be reprogrammed, eliminating the expense of throwing away one-time programmable devices during development and field upgrades (see Figure 15 for the flash memory sector maps). Flash memory can be password protected with a 16-word key, denying access to program memory by unauthorized individuals.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

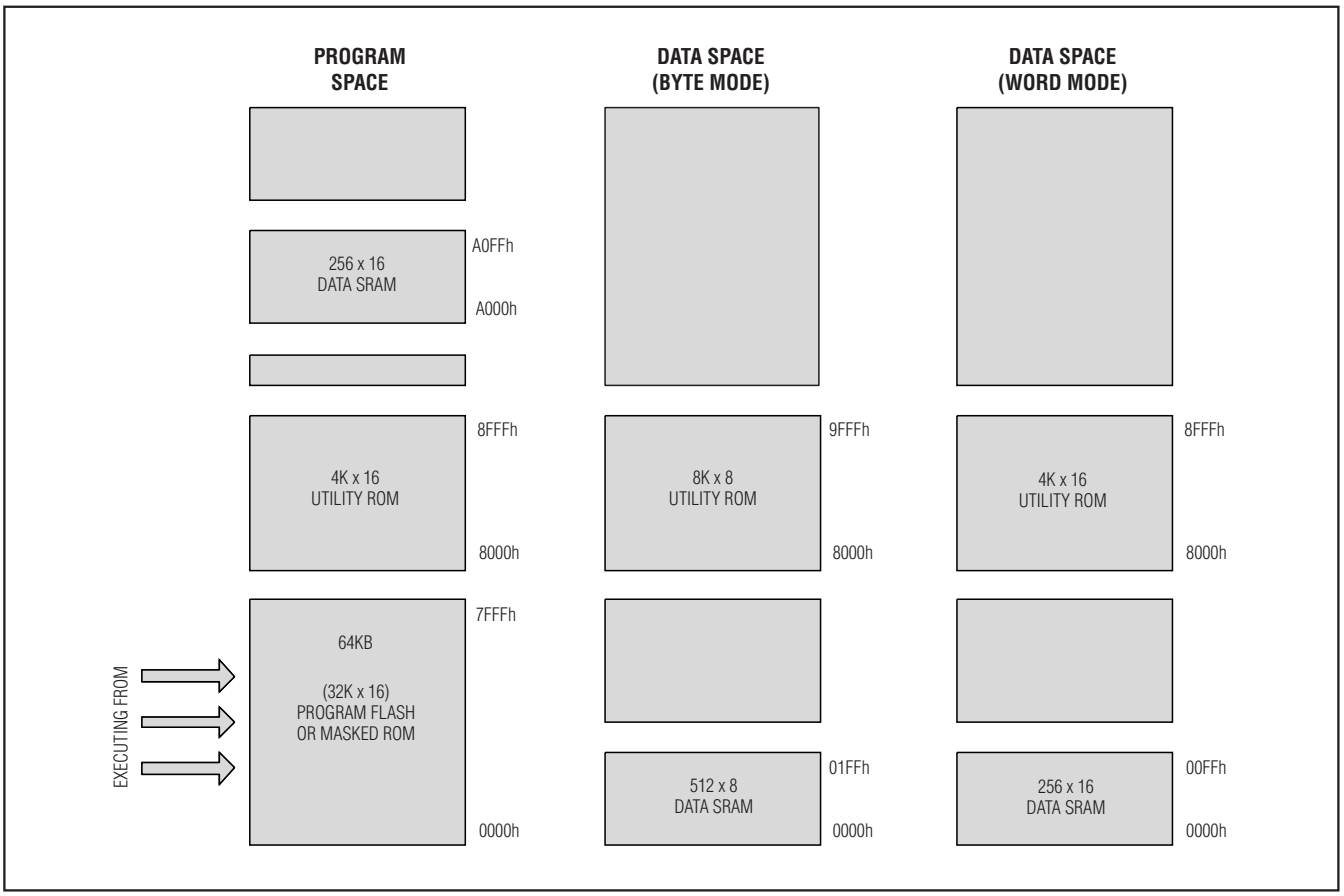


Figure 14. MAXQ7665B Memory Map

A pseudo-Von Neumann memory map can also be enabled. This places the utility ROM, code, and data memory into a single contiguous memory map. This is useful for applications that require dynamic program modification or unique memory configurations.

Stack Memory

A 16-bit-wide x 16 deep internal hardware stack provides storage for program return addresses and general-purpose use. The stack is used automatically by the processor when the CALL, RET, and RETI instructions are executed and interrupts serviced. The stack can also be used explicitly to store and retrieve data by using the PUSH, POP, and POPI instructions.

On reset, the stack pointer, SP, initializes to the top of the stack (0Fh). The CALL, PUSH, and interrupt-vectoring operations increment SP, then store a value at the location pointed to by SP. The RET, RETI, POP, and POPI operations retrieve the value at SP and then decrement SP.

Utility ROM

The utility ROM is an 8KB (4K x 16) block of internal ROM memory that defaults to a starting address of 8000h. The utility ROM consists of subroutines that can be called from application software. These include:

- In-system programming (bootstrap loader) over JTAG
- In-circuit debug routines
- User-callable routines for in-application flash programming and fast table lookup

Following any reset, execution begins in the utility ROM. The ROM software determines whether the program execution should immediately jump to location 0000h, the start of user-application code, or to one of the special routines mentioned. Routines within the utility ROM are user-accessible and can be called as subroutines by the application software. More information on the utility ROM contents is contained in the *MAXQ7665/MAXQ7666 User's Guide*.

Some applications require protection against unauthorized viewing of program code memory. For these applications, access to in-system programming, in-application programming, or in-circuit debugging functions is prohibited until a password has been supplied. The password is defined as the 16 words of physical program memory at addresses 0010h to 001Fh.

A single password lock (PWL) bit is implemented in the SC register. When the PWL is set to one (POR default), the password is required to access the utility ROM, including in-circuit debug and in-system programming routines that allow reading or writing of internal memory. When PWL is cleared to zero, these utilities are fully accessible without the password. The password is automatically set to all ones following a mass erase.

Programming

The flash memory of the µC can be programmed by two different methods: in-system programming and in-application programming. Both methods afford great flexibility in system design as well as reduce the lifecycle cost of the embedded system. These features can be password protected to prevent unauthorized access to program memory.

In-System Programming

An internal bootstrap loader allows the device to be reloaded over a simple JTAG interface. As a result, software can be upgraded in-system, eliminating the need for a costly hardware retrofit when updates are required. Remote software uploads are possible that enable physically inaccessible applications to be frequently updated. The interface hardware can be a JTAG connection to another µC, or a connection to a PC serial port using a serial-to-JTAG converter such as the MAXQJTAG-001, available from Maxim Integrated Products, Inc. If in-system programmability is not required, a commercial gang programmer can be used for mass programming.

After a power-up or reset, the JTAG interface is active and loading the TAP with the system programming instruction invokes the bootstrap loader. Setting the SPE bit to 1 during reset through the JTAG interface executes the bootstrap-loader-mode program that resides in the utility ROM. When programming is complete, the bootstrap loader can clear the SPE bit and reset the device, allowing the device to bypass the utility ROM and begin execution of the application software.

The following bootstrap loader functions are supported:

- Load
- Dump
- CRC
- Verify
- Erase

In-Application Programming

The in-application programming feature allows the µC to modify its own flash program memory while simultaneously executing its application software. This allows on-the-fly software updates in mission-critical applications that cannot afford downtime. Alternatively, it allows the application to develop custom loader software that can operate under the control of the application software. The utility ROM contains user-accessible flash programming functions that erase and program flash memory. These functions are described in detail in the *MAXQ7665/MAXQ7666 User's Guide* for these devices.

Register Set

Most functions of these devices are controlled by sets of registers. These registers provide a working space for memory operations as well as configuring and addressing peripheral registers on the device. Registers are divided into two major types: system registers and peripheral registers. The common register set, also known as the system registers, includes the ALU, accumulator registers, data pointers, interrupt vectors and control, and stack pointer. The peripheral registers define additional functionality that may be included by different products based on the MAXQ architecture. This functionality is broken up into discrete modules so that only the features required for a given product need to be included. Tables 2 and 4 show the MAXQ7665A–MAXQ7665D register set. Tables 3 and 5 show the bit functions and reset values.

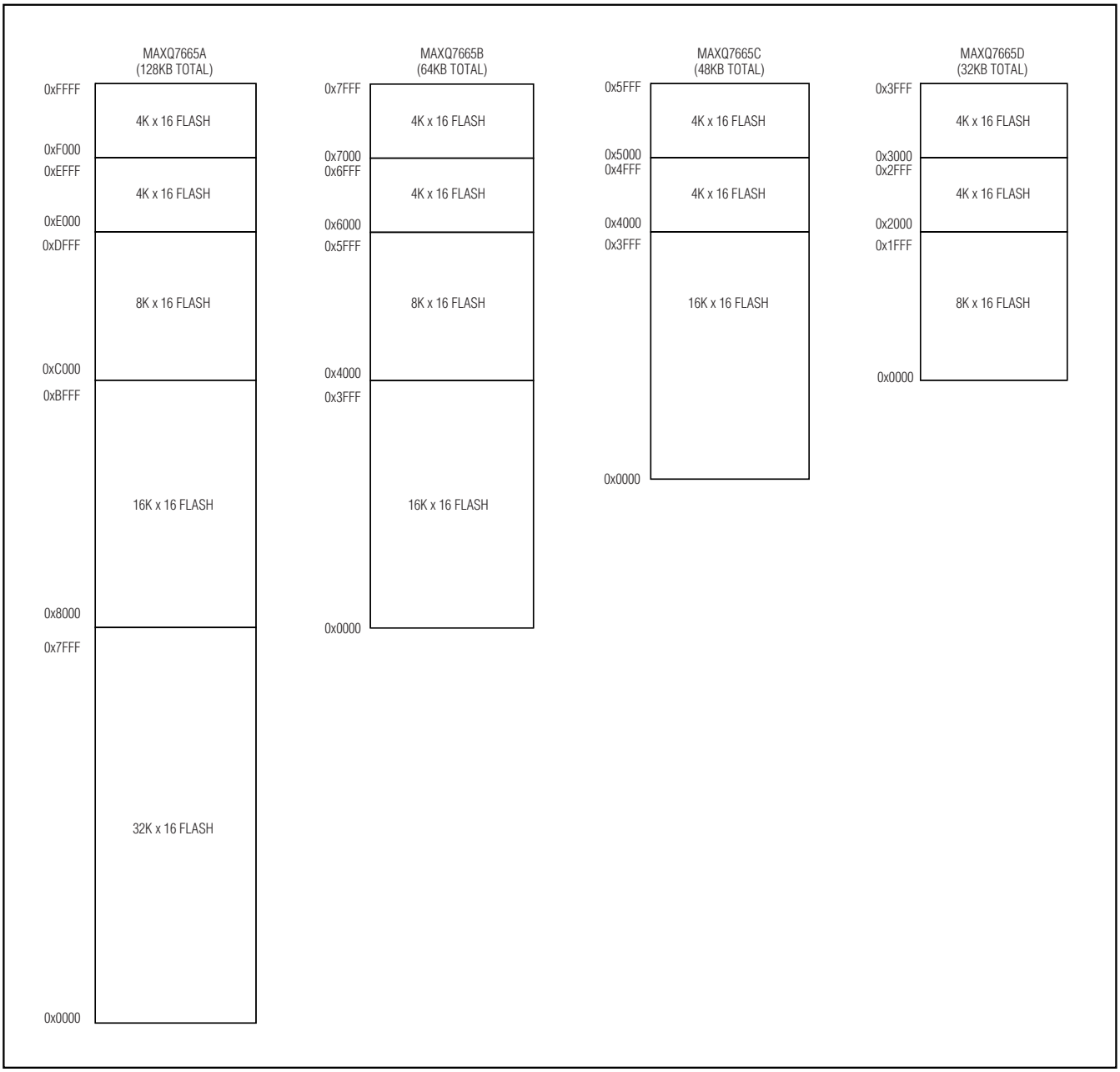


Figure 15. Flash Memory Sector Maps

Power Management

Advanced power-management features minimize power consumption by dynamically matching the processing speed of the device to the required performance level. This means device operation can be slowed and power consumption minimized during periods of reduced activity. When more processing power is required, the µC can increase its operating frequency. Software-selectable clock-divide operations allow flexibility, selecting whether a system clock cycle is one, two, four, or eight oscillator cycles. By performing this function in software, a lower power state can be entered without the cost of additional hardware.

For extremely power-sensitive applications, two additional low-power modes are available:

- PMM: divide-by-256 power-management mode (PMME = 1, CD1:0 = 00b)
- Stop mode (STOP = 1)

In PMM, one system clock is 256 oscillator cycles, significantly reducing power consumption while the µC functions at reduced speed. The optional switchback feature allows enabled interrupt sources including external interrupts, UART, and CAN, to quickly exit the power-management mode and return to a faster internal clock rate.

Power consumption reaches its minimum in stop mode. In this mode, the external oscillator, internal RC oscillator, system clock, and all processing activity is halted. Stop mode is exited when an enabled external interrupt input is triggered or an external reset signal is applied to $\overline{\text{RESET}}$. Upon exiting stop mode, the µC can choose to wait for the external high-frequency crystal to complete its warmup period, or it can start execution immediately from its internal RC oscillator while the warmup period completes.

Table 2. System Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)						
	AP (8h)	**A (9h)**	**PFX (Bh)**	**IP (Ch)**	**SP (Dh)**	**DPC (Eh)**	**DP (Fh)**
0h	AP	**A[0]**	**PFX[0]**	**IP**	—	—	—
1h	APC	**A[1]**	**PFX[1]**	—	**SP**	—	—
2h	—	**A[2]**	**PFX[2]**	—	**IV**	—	—
3h	—	**A[3]**	**PFX[3]**	—	—	OFFS	**DP0**
4h	PSF	**A[4]**	**PFX[4]**	—	—	**DPC**	—
5h	IC	**A[5]**	**PFX[5]**	—	—	**GR**	—
6h	IMR	**A[6]**	**PFX[6]**	—	**LC0**	GRL	—
7h	—	**A[7]**	**PFX[7]**	—	**LC1**	**BP**	**DP1**
8h	SC	**A[8]**		—	—	***GRS***	—
9h	—	**A[9]**	—	—	—	GRH	—
Ah	—	**A[10]**	—	—	—	***GRXL***	—
Bh	*IIR*	**A[11]**	—	—	—	***FP***	—
Ch	—	**A[12]**	—	—	—	—	—
Dh	—	**A[13]**	—	—	—	—	—
Eh	CKCN	**A[14]**	—	—	—	—	—
Fh	WDCN	**A[15]**	—	—	—	—	—

Note: Names that appear in italics indicate that all bits of a register are read-only. Names that appear in bold indicate that a register is 16 bits wide.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Interrupts

Multiple interrupt sources are available for quick response to internal and external events. The MAXQ architecture uses a single interrupt vector (IV), single interrupt-service routine (ISR) design. For maximum flexibility, interrupts can be enabled globally, individually, or by module. When an interrupt condition occurs, its individual flag is set, even if the interrupt source is disabled at the local, module, or global level. Interrupt flags must be cleared within the user-interrupt routine to avoid repeated false interrupts from the same source. Application software must ensure a delay between the write to the flag and the RETI instruction to allow time for the interrupt hardware to remove the internal interrupt condition. Asynchronous interrupt flags require a one-instruction delay and synchronous interrupt flags require a two-instruction delay.

When an enabled interrupt is detected, software jumps to a user-programmable interrupt vector location. The IV register defaults to 0000h on reset or power-up, so if it is not changed to a different address, the user program must determine whether a jump to 0000h came from a reset or interrupt source.

Once software control has been transferred to the ISR, the interrupt identification register (IIR) can be used to determine if a system register or peripheral register was the source of the interrupt. The specified module can then be interrogated for the specific interrupt source and software can take appropriate action. Because the interrupts are evaluated by user software, the user can define a unique interrupt priority scheme for each application. The following interrupt sources are available.

- Watchdog interrupt
- External interrupts 0 to 7
- Serial port 0 receive and transmit interrupts
- Timer 0 low compare, low overflow, capture/compare, and overflow interrupts
- Timer 1 low compare, low overflow, capture/compare, and overflow interrupts
- Timer 2 low compare, low overflow, and overflow interrupts
- CAN0 receive and transmit interrupts and a change in CAN0 status register interrupt
- ADC data ready and overrun interrupts
- Digital and I/O voltage brownout interrupts
- High-frequency oscillator failure interrupt

Reset Sources

Several reset sources are provided for µC control. Although code execution is halted in the reset state, the high-frequency oscillators and the internal RC oscillator continue to oscillate. The high-frequency oscillator is turned off by a POR, but not by other reset sources. Internal resets such as the power-on and watchdog resets assert the $\overline{\text{RESET}}$ output low.

Power-On Reset (POR)

An internal POR circuit enhances system reliability. This circuit forces the device to perform a POR whenever a rising voltage on DV_{DD} climbs above the POR threshold level of 2.7V. At this point the following events occur:

- All registers and circuits enter their reset state
- The POR flag (WDCN.POR) is set to indicate the source of the reset
- The internal RC oscillator becomes the clock source
- Code execution begins at location 8000h

Watchdog Timer Reset

The watchdog timer functions are described in the *MAXQ7665/MAXQ7666 User's Guide*. Execution resumes at location 8000h following a watchdog timer reset.

External System Reset

Asserting the external $\overline{\text{RESET}}$ input low causes the device to enter the reset state. The external reset functions as described in the *MAXQ7665/MAXQ7666 User's Guide*. Execution resumes at location 8000h after $\overline{\text{RESET}}$ is released.

Crystal Selection

The MAXQ7665A–MAXQ7665D require a crystal with the following specifications:

Frequency: 1MHz to 8MHz

C_{LOAD}: 6pF (min)

Drive level: 5µW

Series resonance resistance: 30Ω max

Note: Series resonance resistance is the resistance observed when the resonator is in the series resonant condition. This is a parameter often stated by quartz crystal vendors and is called R1. When a resonator is used in the parallel resonant mode with an external load capacitance, as is the case with the MAXQ7665A–MAXQ7665D oscillator circuit, the effective resistance is sometimes stated. This effective resistance at the loaded frequency of oscillation is:

$$R1 \times (1 + (C_O/C_{LOAD}))^2$$

For typical C_O and C_{LOAD} values, the effective resistance can be greater than R1 by a factor of 2.

Development and Technical Support

A variety of highly versatile, affordably priced development tools for this µC are available from Maxim and third-party suppliers, including:

- Compilers
- Evaluation kits
- Integrated development environments (IDEs)
- JTAG-to-serial converters for programming and debugging

A list of some development-tool vendors can be found at **www.maxim-ic.com/microcontrollers**.

Technical support is available through email at maxq.support@maxim-ic.com.

Table 3. System Register Bit Functions and Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
AP									—	—	—	—	AP (4 Bits)			
									0	0	0	0	0	0	0	0
APC									CLR	IDS	—	—	—	MOD2	MOD1	MOD0
									0	0	0	0	0	0	0	0
PSF									Z	S	—	GPF1	GPF0	OV	C	E
									1	0	0	0	0	0	0	0
IC									—	—	CGDS	—	—	—	INS	IGE
									0	0	0	0	0	0	0	0
IMR									IMS	—	IM5	IM4	IM3	IM2	IM1	IM0
									0	0	0	0	0	0	0	0
SC									TAP	—	CDA1	CDA0	UPA	ROD	PWL	—
									1	0	0	0	0	0	s*	0
IIR									IIS	—	II5	II4	II3	II2	II1	II0
									0	0	0	0	0	0	0	0
CKCN									XT	—	RGMD	STOP	SWB	PMME	CD1	CD0
									s*	0	s*	0	0	0	0	1
WDCN									POR	EWDI	WD1	WD0	WDIF	WTRF	EWT	RWT
									s*	s*	0	0	0	s*	s*	0
A[n] (0..15)	A[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PFX[n] (0..15)	PFX[n] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
IP	IP (16 Bits)															
	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SP	—	—	—	—	—	—	—	—	—	—	—	—	SP (4 Bits)			
	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
IV	IV (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[0]	LC[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
LC[1]	LC[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OFFS									OFFS (8 Bits)							
									0	0	0	0	0	0	0	0
DPC	—	—	—	—	—	—	—	—	—	—	—	WBS2	WBS1	WBS0	SDPS1	SDPS0
	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0
GR	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRL									GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
									0	0	0	0	0	0	0	0
BP	BP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRS	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0	GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
GRH									GR.15	GR.14	GR.13	GR.12	GR.11	GR.10	GR.9	GR.8
									0	0	0	0	0	0	0	0
GRXL	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.7	GR.6	GR.5	GR.4	GR.3	GR.2	GR.1	GR.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FP	FP (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[0]	DP[0] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DP[1]	DP[1] (16 Bits)															
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

**Bits indicated by an "s" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR. Refer to the MAXQ7665/MAXQ7666 User's Guide for more information.*

Table 4. Peripheral Register Map

REGISTER INDEX	MODULE NAME (BASE SPECIFIER)					
	M0 (0h)	**M1 (1h)**	**M2 (2h)**	**M3 (3h)**	**M4 (4h)**	**M5 (5h)**
0h	PO0	MCNT	T2CNA0	T2CNA2	C0C	VMC
1h	—	MA	T2H0	T2H2	C0S	APE
2h	—	MB	T2RH0	T2RH2	**C0IR**	ACNT
3h	EIF0	MC2	T2CH0	T2CH2	C0TE	DCNT
4h	—	MC1	T2CNA1	—	C0RE	DACI
5h	—	MC0	T2H1	—	COR	—
6h	—	—	T2RH1	—	C0DP	DACO
7h	SBUF0	—	T2CH1	—	C0DB	—
8h	**PI0**	—	T2BNB0	T2CNB2	**C0RMS**	**ADCD**
9h	—	—	T2V0	T2V2	**C0TMA**	**TSO**
Ah	—	FCNTL	T2R0	T2R2	—	AIE
Bh	EIE0	FDATA	*T2C0*	T2C2	—	**ASR**
Ch	—	**MC1R**	T2CNB1	—	—	OSCC
Dh	—	**MC0R**	T2V1	—	—	—
Eh	—	—	T2R1	—	—	—
Fh	—	—	T2C1	—	—	—
10h	PD0	—	T2CFG0	T2CFG2	—	—
11h	—	—	T2CFG1	—	C0M1C	—
12h	—	—	—	—	C0M2C	—
13h	EIES0	—	—	—	C0M3C	—
14h	—	—	—	—	C0M4C	—
15h	—	—	—	—	C0M5C	—
16h	—	—	—	—	C0M6C	—
17h	—	—	—	—	C0M7C	—
18h	—	—	ICDT0	—	C0M8C	—
19h	—	—	ICDT1	—	C0M9C	—
1Ah	—	—	ICDC	—	C0M10C	—
1Bh	—	—	ICDF	—	C0M11C	—
1Ch	—	Reserved	ICDB	—	C0M12C	—
1Dh	SCON0	—	ICDA	—	C0M13C	—
1Eh	SMD0	—	ICDD	—	C0M14C	—
1Fh	PR0	—	—	—	C0M15C	—

Note: *Names that appear in bold indicate that the register is read-only.*

Table 5. Peripheral Register Bit Functions and Reset Values

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
PO0	—	—	—	—	—	—	—	—	PO0.7	PO0.6	PO0.5	PO0.4	PO0.3	PO0.2	PO0.1	PO0.0
(M0, 0h)	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
EIF0	—	—	—	—	—	—	—	—	IE7	IE6	IE5	IE4	IE3	IE2	IE1	IE0
(M0, 3h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SBUF0	—	—	—	—	—	—	—	—	SBUF0.7	SBUF0.6	SBUF0.5	SBUF0.4	SBUF0.3	SBUF0.2	SBUF0.1	SBUF0.0
(M0, 7h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PI0	—	—	—	—	—	—	—	—	PI0.7	PI0.6	PI0.5	PI0.4	PI0.3	PI0.2	PI0.1	PI0.0
(M0, 8h)	0	0	0	0	0	0	0	0	ST	ST	ST	ST	ST	ST	ST	ST
EIE0	—	—	—	—	—	—	—	—	EX7	EX6	EX5	EX4	EX3	EX2	EX1	EX0
(M0, Bh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PD0	—	—	—	—	—	—	—	—	PD0.7	PD0.6	PD0.5	PD0.4	PD0.3	PD0.2	PD0.1	PD0.0
(M0, 10h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
EIES0	—	—	—	—	—	—	—	—	IT7	IT6	IT5	IT4	IT3	IT2	IT1	IT0
(M0, 13h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SCON0	—	—	—	—	—	—	—	—	SM0/FE	SM1	SM2	REN	TB8	RB8	TI	RI
(M0, 1Dh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
SMD0	—	—	—	—	—	—	—	—	—	—	—	—	—	ESI	SMOD	FEDE
(M0, 1Eh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
PR0	PR0.15	PR0.14	PR0.13	PR0.12	PR0.11	PR0.10	PR0.9	PR0.8	PR0.7	PR0.6	PR0.5	PR0.4	PR0.3	PR0.2	PR0.1	PR0.0
(M0, 1Fh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MCNT	—	—	—	—	—	—	—	—	OF	MCW	CLD	SQU	OPCS	MSUB	MMAC	SUS
(M1, 0h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MA	MA.15	MA.14	MA.13	MA.12	MA.11	MA.10	MA.9	MA.8	MA.7	MA.6	MA.5	MA.4	MA.3	MA.2	MA.1	MA.0
(M1, 1h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MB	MB.15	MB.14	MB.13	MB.12	MB.11	MB.10	MB.9	MB.8	MB.7	MB.6	MB.5	MB.4	MB.3	MB.2	MB.1	MB.0
(M1, 2h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MC2	MC2.15	MC2.14	MC2.13	MC2.12	MC2.11	MC2.10	MC2.9	MC2.8	MC2.7	MC2.6	MC2.5	MC2.4	MC2.3	MC2.2	MC2.1	MC2.0
(M1, 3h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MC1	MC1.15	MC1.14	MC1.13	MC1.12	MC1.11	MC1.10	MC1.9	MC1.8	MC1.7	MC1.6	MC1.5	MC1.4	MC1.3	MC1.2	MC1.1	MC1.0
(M1, 4h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MC0	MC0.15	MC0.14	MC0.13	MC0.12	MC0.11	MC0.10	MC0.9	MC0.8	MC0.7	MC0.6	MC0.5	MC0.4	MC0.3	MC0.2	MC0.1	MC0.0
(M1, 5h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
FCNTL	—	—	—	—	—	—	—	—	FBUSY	FERR	FINE	FBYP	DQ5	FC2	FC1	—
(M1, Ah)	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
FDATA	FDATA.15	FDATA.14	FDATA.13	FDATA.12	FDATA.11	FDATA.10	FDATA.9	FDATA.8	FDATA.7	FDATA.6	FDATA.5	FDATA.4	FDATA.3	FDATA.2	FDATA.1	FDATA.0
(M1, Bh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MC1R	MC1R.15	MC1R.14	MC1R.13	MC1R.12	MC1R.11	MC1R.10	MC1R.9	MC1R.8	MC1R.7	MC1R.6	MC1R.5	MC1R.4	MC1R.3	MC1R.2	MC1R.1	MC1R.0
(M1, Ch)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
MC0R	MC0R.15	MC0R.14	MC0R.13	MC0R.12	MC0R.11	MC0R.10	MC0R.9	MC0R.8	MC0R.7	MC0R.6	MC0R.5	MC0R.4	MC0R.3	MC0R.2	MC0R.1	MC0R.0
(M1, Dh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA0	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
(M2, Oh)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H0	—	—	—	—	—	—	—	—	T2H0.7	T2H0.6	T2H0.5	T2H0.4	T2H0.3	T2H0.2	T2H0.1	T2H0.0
(M2, 1h)	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTERED BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T2RH0 (M2, 2h)	—	—	—	—	—	—	—	—	T2RH0.7	T2RH0.6	T2RH0.5	T2RH0.4	T2RH0.3	T2RH0.2	T2RH0.1	T2RH0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH0 (M2, 3h)	—	—	—	—	—	—	—	—	T2CH0.7	T2CH0.6	T2CH0.5	T2CH0.4	T2CH0.3	T2CH0.2	T2CH0.1	T2CH0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA1 (M2, 4h)	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H1 (M2, 5h)	—	—	—	—	—	—	—	—	T2H1.7	T2H1.6	T2H1.5	T2H1.4	T2H1.3	T2H1.2	T2H1.1	T2H1.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH1 (M2, 6h)	—	—	—	—	—	—	—	—	T2RH1.7	T2RH1.6	T2RH1.5	T2RH1.4	T2RH1.3	T2RH1.2	T2RH1.1	T2RH1.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH1 (M2, 7h)	—	—	—	—	—	—	—	—	T2CH1.7	T2CH1.6	T2CH1.5	T2CH1.4	T2CH1.3	T2CH1.2	T2CH1.1	T2CH1.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB0 (M2, 8h)	—	—	—	—	—	—	—	—	ET2L	—	—	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V0 (M2, 9h)	T2V0.15	T2V0.14	T2V0.13	T2V0.12	T2V0.11	T2V0.10	T2V0.9	T2V0.8	T2V0.7	T2V0.6	T2V0.5	T2V0.4	T2V0.3	T2V0.2	T2V0.1	T2V0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R0 (M2, Ah)	T2R0.15	T2R0.14	T2R0.13	T2R0.12	T2R0.11	T2R0.10	T2R0.9	T2R0.8	T2R0.7	T2R0.6	T2R0.5	T2R0.4	T2R0.3	T2R0.2	T2R0.1	T2R0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C0 (M2, Bh)	T2C0.15	T2C0.14	T2C0.13	T2C0.12	T2C0.11	T2C0.10	T2C0.9	T2C0.8	T2C0.7	T2C0.6	T2C0.5	T2C0.4	T2C0.3	T2C0.2	T2C0.1	T2C0.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNB1 (M2, Ch)	—	—	—	—	—	—	—	—	ET2L	—	—	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V1 (M2, Dh)	T2V1.15	T2V1.14	T2V1.13	T2V1.12	T2V1.11	T2V1.10	T2V1.9	T2V1.8	T2V1.7	T2V1.6	T2V1.5	T2V1.4	T2V1.3	T2V1.2	T2V1.1	T2V1.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R1 (M2, Eh)	T2R1.15	T2R1.14	T2R1.13	T2R1.12	T2R1.11	T2R1.10	T2R1.9	T2R1.8	T2R1.7	T2R1.6	T2R1.5	T2R1.4	T2R1.3	T2R1.2	T2R1.1	T2R1.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C1 (M2, Fh)	T2C1.15	T2C1.14	T2C1.13	T2C1.12	T2C1.11	T2C1.10	T2C1.9	T2C1.8	T2C1.7	T2C1.6	T2C1.5	T2C1.4	T2C1.3	T2C1.2	T2C1.1	T2C1.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG0 (M2, 10h)	—	—	—	—	—	—	—	—	—	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG1 (M2, 11b)	—	—	—	—	—	—	—	—	—	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDT0 (M2, 18h)	ICDT0.15	ICDT0.14	ICDT0.13	ICDT0.12	ICDT0.11	ICDT0.10	ICDT0.9	ICDT0.8	ICDT0.7	ICDT0.6	ICDT0.5	ICDT0.4	ICDT0.3	ICDT0.2	ICDT0.1	ICDT0.0
	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDT1 (M2, 19h)	ICDT1.15	ICDT1.14	ICDT1.13	ICDT1.12	ICDT1.11	ICDT1.10	ICDT1.9	ICDT1.8	ICDT1.7	ICDT1.6	ICDT1.5	ICDT1.4	ICDT1.3	ICDT1.2	ICDT1.1	ICDT1.0
	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB	DB
ICDC (M2, 1Ah)	—	—	—	—	—	—	—	—	DME	—	REGE	—	CMD3	CMD2	CMD1	CMD0
	0	0	0	0	0	0	0	0	DW	0	DW	0	DW	DW	DW	DW
ICDF (M2, 1Bh)	—	—	—	—	—	—	—	—	—	—	—	—	PSS1	PSS0	SPE	TXC
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDB (M2, 1Ch)	—	—	—	—	—	—	—	—	ICDB.7	ICDB.6	ICDB.5	ICDB.4	ICDB.3	ICDB.2	ICDB.1	ICDB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDA M2, 1Dh)	ICDA.15	ICDA.14	ICDA.13	ICDA.12	ICDA.11	ICDA.10	ICDA.9	ICDA.8	ICDA.7	ICDA.6	ICDA.5	ICDA.4	ICDA.3	ICDA.2	ICDA.1	ICDA.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ICDD (M2, 1Eh)	ICDD.15	ICDD.14	ICDD.13	ICDD.12	ICDD.11	ICDD.10	ICDD.9	ICDD.8	ICDD.7	ICDD.6	ICDD.5	ICDD.4	ICDD.3	ICDD.2	ICDD.1	ICDD.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CNA2 (M3, 0h)	—	—	—	—	—	—	—	—	ET2	T2OE0	T2POL0	TR2L	TR2	CPRL2	SS2	G2EN
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2H2 (M3, 1h)	—	—	—	—	—	—	—	—	T2H2.7	T2H2.6	T2H2.5	T2H2.4	T2H2.3	T2H2.2	T2H2.1	T2H2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2RH2 (M3, 2h)	—	—	—	—	—	—	—	—	T2RH2.7	T2RH2.6	T2RH2.5	T2RH2.4	T2RH2.3	T2RH2.2	T2RH2.1	T2RH2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CH2 (M3, 3h)	—	—	—	—	—	—	—	—	T2CH2.7	T2CH2.6	T2CH2.5	T2CH2.4	T2CH2.3	T2CH2.2	T2CH2.1	T2CH2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
T2CNB2 (M3, 8h)	—	—	—	—	—	—	—	—	ET2L	—	—	—	TF2	TF2L	TCC2	TC2L
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2V2 (M3, 9h)	T2V2.15	T2V2.14	T2V2.13	T2V2.12	T2V2.11	T2V2.10	T2V2.9	T2V2.8	T2V2.7	T2V2.6	T2V2.5	T2V2.4	T2V2.3	T2V2.2	T2V2.1	T2V2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2R2 (M3, Ah)	T2R2.15	T2R2.14	T2R2.13	T2R2.12	T2R2.11	T2R2.10	T2R2.9	T2R2.8	T2R2.7	T2R2.6	T2R2.5	T2R2.4	T2R2.3	T2R2.2	T2R2.1	T2R2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2C2 (M3, Dh)	T2C2.15	T2C2.14	T2C2.13	T2C2.12	T2C2.11	T2C2.10	T2C2.9	T2C2.8	T2C2.7	T2C2.6	T2C2.5	T2C2.4	T2C2.3	T2C2.2	T2C2.1	T2C2.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
T2CFG2 (M3, 10h)	—	—	—	—	—	—	—	—	—	T2DIV2	T2DIV1	T2DIV0	T2MD	CCF1	CCF0	C/T2
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0C (M4, 0h)	—	—	—	—	—	—	—	—	ERIE	STIE	PDE	SIESTA	CRST	AUTOB	ERCS	SWINT
	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	1
C0S (M4, 1h)	—	—	—	—	—	—	—	—	BSS	EC96/128	WKS	RXS	TXS	ER2	ER1	ER0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0IR (M4, 2h)	—	—	—	—	—	—	—	—	INTIN7	INTIN6	INTIN5	INTIN4	INTIN3	INTIN2	INTIN1	INTIN0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TE (M4, 3h)	—	—	—	—	—	—	—	—	C0TE.7	C0TE.6	C0TE.5	C0TE.4	C0TE.3	C0TE.2	C0TE.1	C0TE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RE (M4, 4h)	—	—	—	—	—	—	—	—	C0RE.7	C0RE.6	C0RE.5	C0RE.4	C0RE.3	C0RE.2	C0RE.1	C0RE.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0R (M4, 5h)	—	—	—	—	—	—	—	—	CAN0BA	INCDEC	AID	C0BPR7	C0BPR6	—	C0BIE	C0IE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DP (M4, 6h)	C0DP.15	C0DP.14	C0DP.13	C0DP.12	C0DP.11	C0DP.10	C0DP.9	C0DP.8	C0DP.7	C0DP.6	C0DP.5	C0DP.4	C0DP.3	C0DP.2	C0DP.1	C0DP.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0DB (M4, 7h)	C0DB.15	C0DB.14	C0DB.13	C0DB.12	C0DB.11	C0DB.10	C0DB.9	C0DB.8	C0DB.7	C0DB.6	C0DB.5	C0DB.4	C0DB.3	C0DB.2	C0DB.1	C0DB.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0RMS (M4, 8h)	—	C0RMS.15	C0RMS.14	C0RMS.13	C0RMS.12	C0RMS.11	C0RMS.10	C0RMS.9	C0RMS.8	C0RMS.7	C0RMS.6	C0RMS.5	C0RMS.4	C0RMS.3	C0RMS.2	C0RMS.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0TMA (M4, 9h)	—	C0TMA.15	C0TMA.14	C0TMA.13	C0TMA.12	C0TMA.11	C0TMA.10	C0TMA.9	C0TMA.8	C0TMA.7	C0TMA.6	C0TMA.5	C0TMA.4	C0TMA.3	C0TMA.2	C0TMA.1
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M1C (M4, 11h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M2C (M4, 12h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M3C (M4, 13h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M4C (M4, 14h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M5C (M4, 15h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M6C (M4, 16h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M7C (M4, 17h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M8C (M4, 18h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M9C (M4, 19h)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M10C (M4, 1Ah)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M11C (M4, 1Bh)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M12C (M4, 1Ch)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M13C (M4, 1Dh)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0

Table 5. Peripheral Register Bit Functions and Reset Values (continued)

REGISTER	REGISTER BIT															
	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
C0M14C (M4, 1Eh)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
C0M15C (M4, 1Fh)	—	—	—	—	—	—	—	—	MSRDY	ETI	ERI	INTRQ	EXTRQ	MTRQ	ROW/TIH	DTUP
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
VMC (M5, 0h)	—	—	—	—	—	—	—	—	—	—	VIOBI1	VIOBI0	VDBI1	VDBI0	VDBR1	VDBR0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	S	S
APE (M5, 1h)	—	—	—	VIBE	VDBE	VDPE	—	—	PGG2	PGG1	PGG0	TSE	PGAE	—	DACE	ADCE
	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
ACNT (M5, 2h)	ADCMX4	ADCMX3	ADCMX2	ADCMX1	ADCMX0	ADCDIF	ADCBIP	—	—	ADCDUL	—	ADCASD	ADCBY	ADCS2	ADCS1	ADCS0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DCNT (M5, 3h)	—	—	—	—	—	—	—	—	—	DACLD2	DACLD1	DACLD0	—	—	—	—
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DACI (M5, 4h)	—	—	—	—	DACI.11	DACI.10	DACI.9	DACI.8	DACI.7	DACI.6	DACI.5	DACI.4	DACI.3	DACI.2	DACI.1	DACI.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
DACO (M5, 6h)	—	—	—	—	DACO.11	DACO.10	DACO.9	DACO.8	DACO.7	DACO.6	DACO.5	DACO.4	DACO.3	DACO.2	DACO.1	DACO.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
ADCD (M5, 8h)	—	—	—	—	ADCD.11	ADCD.10	ADCD.9	ADCD.8	ADCD.7	ADCD.6	ADCD.5	ADCD.4	ADCD.3	ADCD.2	ADCD.1	ADCD.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
TSO (M5, 9h)	TSO.15	TSO.14	TSO.13	TSO.12	TSO.11	TSO.10	TSO.9	TSO.8	TSO.7	TSO.6	TSO.5	TSO.4	TSO.3	TSO.2	TSO.1	TSO.0
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
AIE (M5, Ah)	—	—	—	—	—	—	—	—	—	HFFIE	VIOBIE	DVBIE	—	AORIE	ADCIE	—
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
ASR (M5, Bh)	VIOLVL	DVLVL	—	—	XHFRY	—	—	—	—	HFFINT	VIOBI	DVBI	—	ADCOV	ADCRY	—
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
OSCC (M5, Ch)	—	—	—	—	HFOC1	HFOC0	HFIC1	HFIC0	ADCCD2	ADCCD1	ADCCD0	—	—	EXTHF	RCE	HFE
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0

Bits indicated by "—" are unused.

Bits indicated by "ST" reflect the input signal state.

Bits indicated by "S" are only affected by a POR and not by other forms of reset. These bits are set to 0 after a POR.

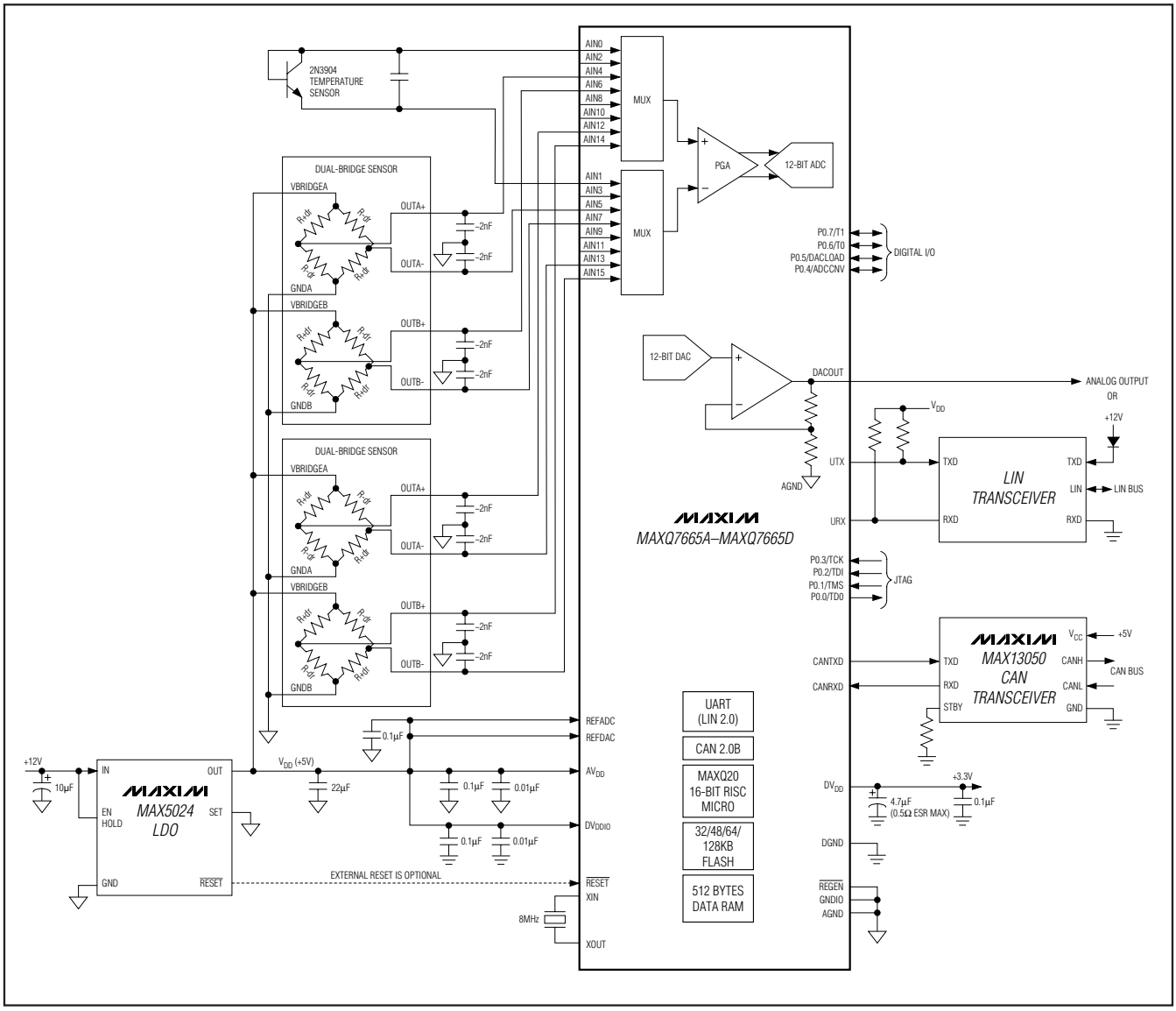
Bits indicated by "DB" have read/write access only in background or debug mode. These bits are cleared after a POR.

Bits indicated by "DW" are only written to in debug mode. These bits are cleared after a POR.

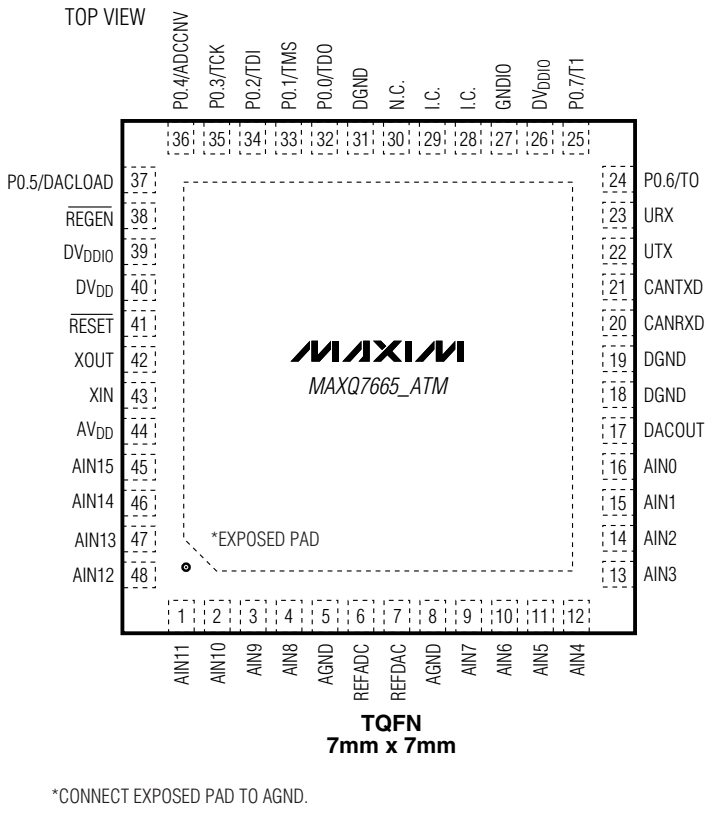
The OSCC register is cleared to 0002h after a POR and is not affected by other forms of reset.

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Typical Operating Circuit



Pin Configuration



TQFN
7mm x 7mm

*CONNECT EXPOSED PAD TO AGND.

Chip Information

PROCESS: BiCMOS and CMOS

16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Ordering Information/Selector Guide

PART	PIN-PACKAGE	PKG CODE	FLASH SIZE (KB)
MAXQ7665AATM+**	48 TQFN-EP*	T4877MK+6	128 (64K x 16)
MAXQ7665BATM+	48 TQFN-EP*	T4877MK+6	64 (32K x 16)
MAXQ7665CATM+**	48 TQFN-EP*	T4877MK+6	48 (24K x 16)
MAXQ7665DATM+**	48 TQFN-EP*	T4877MK+6	32 (16K x 16)

+Devices are only available in lead-free packaging.

**EP = Exposed pad.*

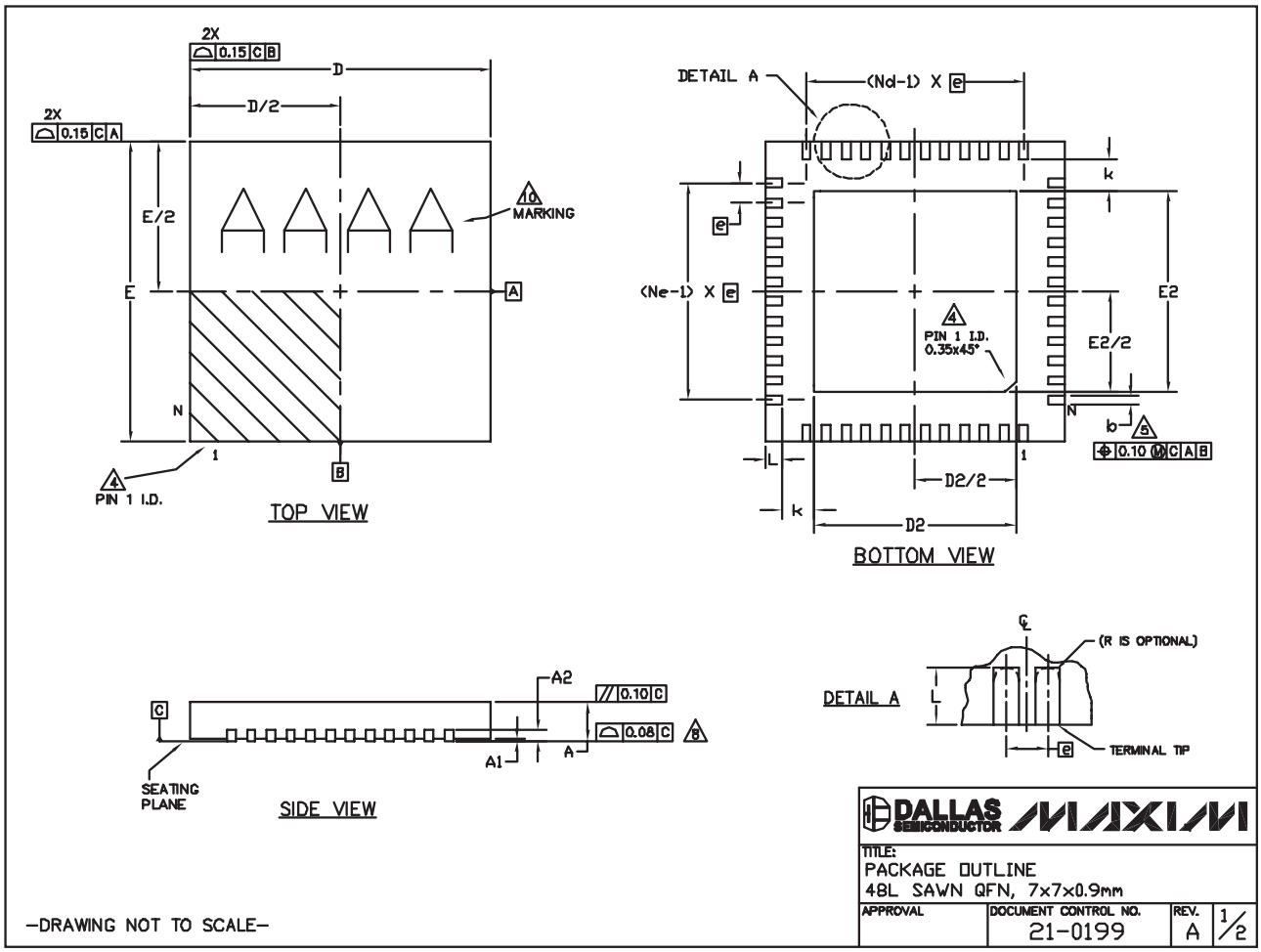
***Future Product—contact factory for availability.*

Note: *All devices are specified for operation over the -40°C to +125°C automotive temperature range.*

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

SAWN QFN.EPS



16-Bit RISC Microcontroller-Based Smart Data-Acquisition Systems

Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. Nd AND Ne REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. WARPAGE SHALL NOT EXCEED 0.10mm.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

DIMENSIONS			
SYMBOL	MIN.	NOM.	MAX.
A	0.80	0.85	0.90
A1	0	0.02	0.05
A2		0.20 REF.	
b	0.20	0.25	0.30
D	6.90	7.00	7.10
E	6.90	7.00	7.10
D2	5.40	5.50	5.60
E2	5.40	5.50	5.60
e		0.50 BSC.	
k	0.25	–	–
L	0.30	0.40	0.50
L1	–	–	–
N		48	
Nd		12	
Ne		12	
Pkg. Code:		T4877MK-6	

–DRAWING NOT TO SCALE–

DALLAS SEMICONDUCTOR MAXIM

TITLE:
PACKAGE OUTLINE
48L SAWN QFN, 7x7x0.9mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
	21-0199	A	2/2